CHAPTER 3

Biasing and Amplifiers

Syllabus

- Basic physics of MOS transistors and their equivalent circuit models (ch. 6)
- Elementary gain stages (ch. 7, ch. 9, and ch. 10)
- Operational amplifier basics (ch. 8)
- Frequency responses (ch. 11)
- Noise (ch.7, Design of analog CMOS ICs)
- Feedback, stability and compensation (ch. 12)
- Operational amplifiers (ch.9, Design of analog CMOS ICs)

Vision

- An important part of a designer's job is to use proper approximations so as to create a simple mental picture of a complicated circuit.

- The intuition thus gained makes it possible to formulate the behavior of most circuits by inspection rather than by lengthy calculations

Basic Concepts

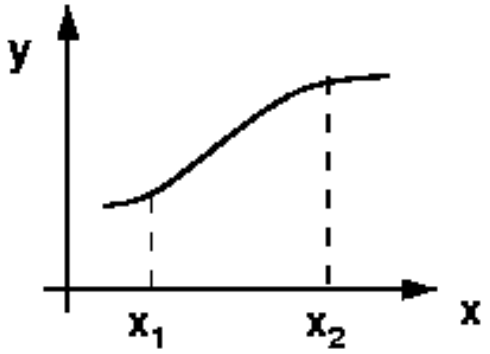
- The input-output characteristic of an amplifier is generally a nonlinear function

$$y(t) \approx \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \cdots + \alpha_n x^n(t) \qquad x_1 \le x \le x_2$$

- For a sufficiently narrow range of *x*

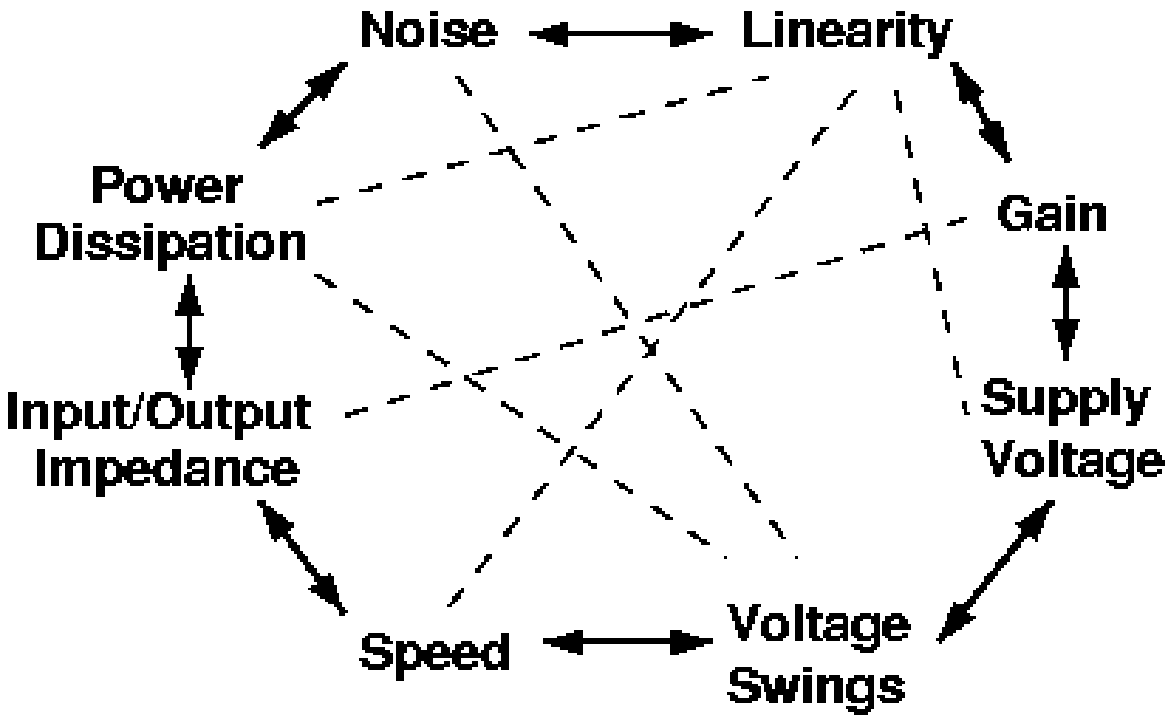
$$y(t) \approx \alpha_0 + \alpha_1 x(t), \quad \alpha_0 : \text{operationg point}, \ \alpha_1 : \text{small signal gain}$$

- As *x(t)* increases in magnitude, higher order terms manifest themselves, leading to nonlinear distortion.
- Input-output characteristic of a nonlinear system



Analog Design Octagon

- Analog design octagon

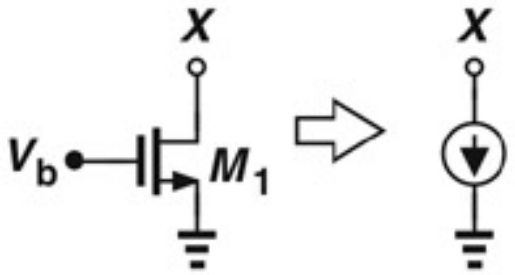


Elementary Gain Stages

- Current Source and Biasing
- CMOS Amplifiers (CS, CG, CD, Cascode)
- Differential Amplifiers

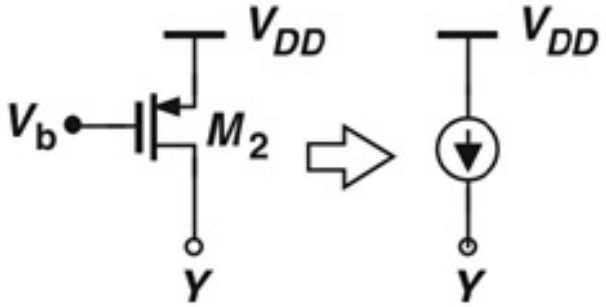
Current Sources

Current sink



An NMOS serves as a current source with one terminal tied to ground

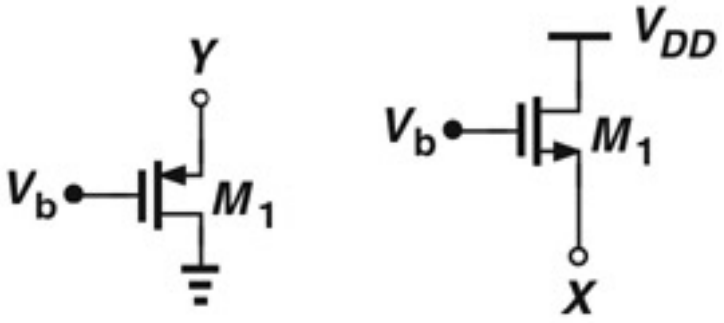
Current source



An PMOS serves as a current source with one terminal tied to V_{DD}

Currents remain independent of V_X or V_Y if $\lambda = 0$ (assume saturation)

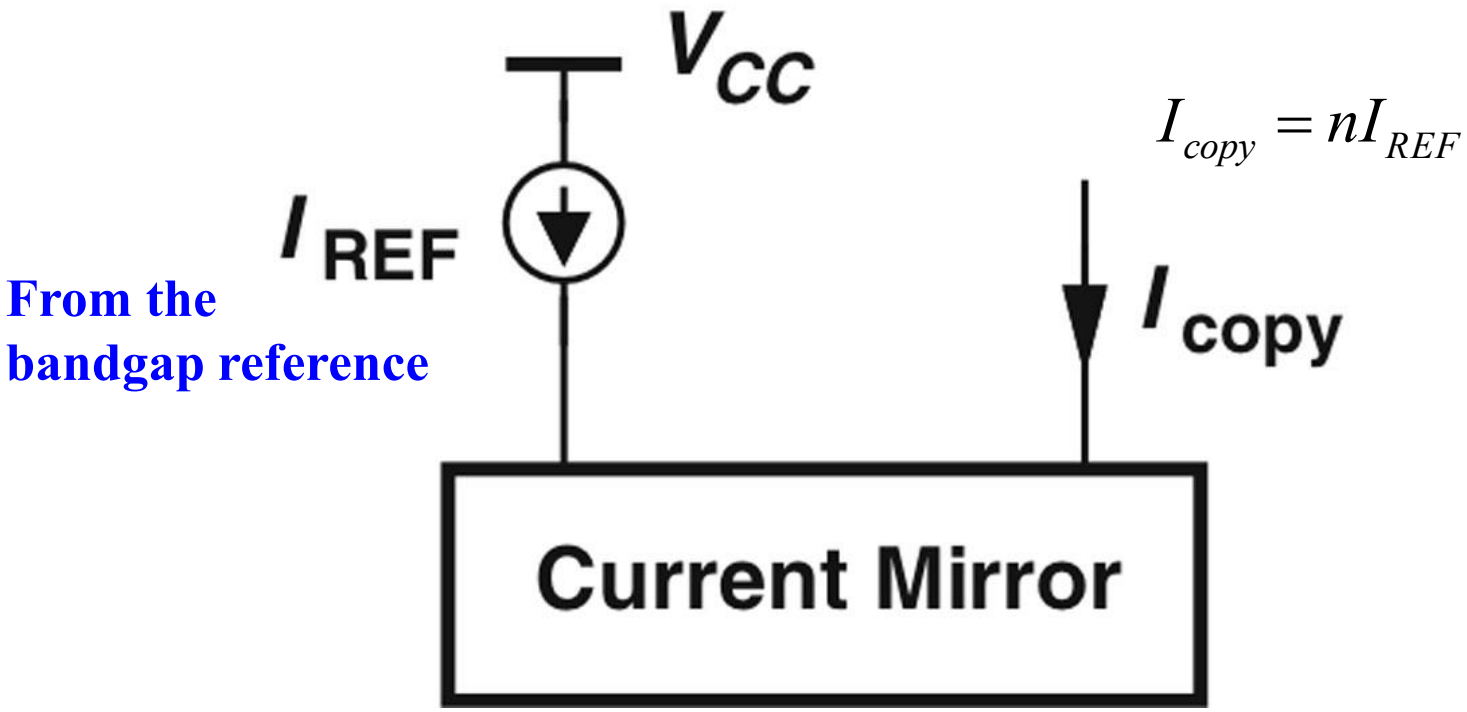
Not operating as current source



- VX and VY directly changes VGS
- Small signal impedance only 1/gm

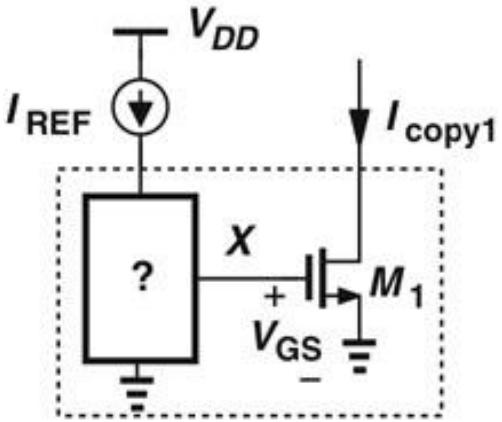
Only the drain terminal can be used!!!

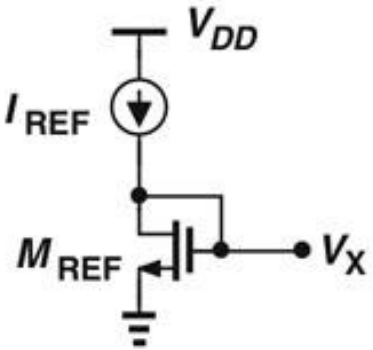
“Copy” the Golden Current

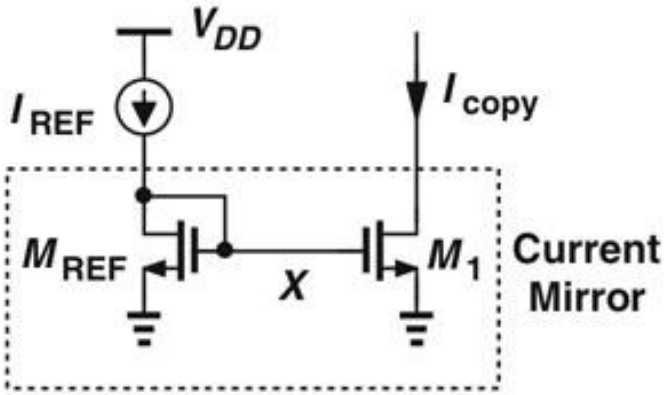


- **The motivation behind a current mirror is to sense the current from a “golden current source” and duplicate this “golden current” to other locations.**

MOSFET Current Mirror







$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_X - V_{TH1})^2 = I_{REF},$$

$$V_X = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH1}.$$

Two ways to look at this:

-M_{REF} takes the square root of I_{REF} and M_1 squares the result

-From the two drain currents:

$$I_{D,REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{REF} (V_X - V_{TH})^2$$

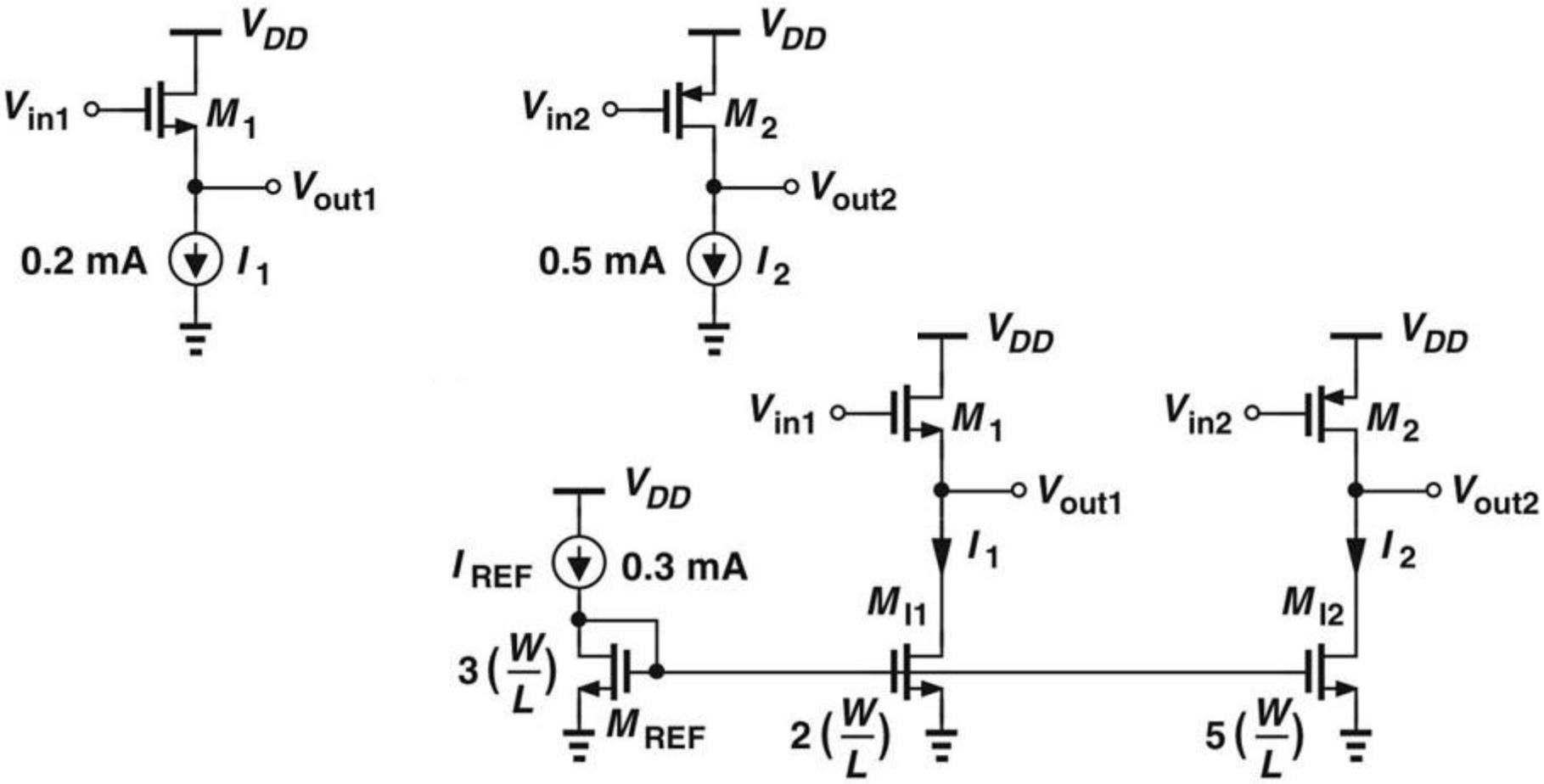
$$I_{copy} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_X - V_{TH})^2,$$

$$\Rightarrow \quad I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF},$$

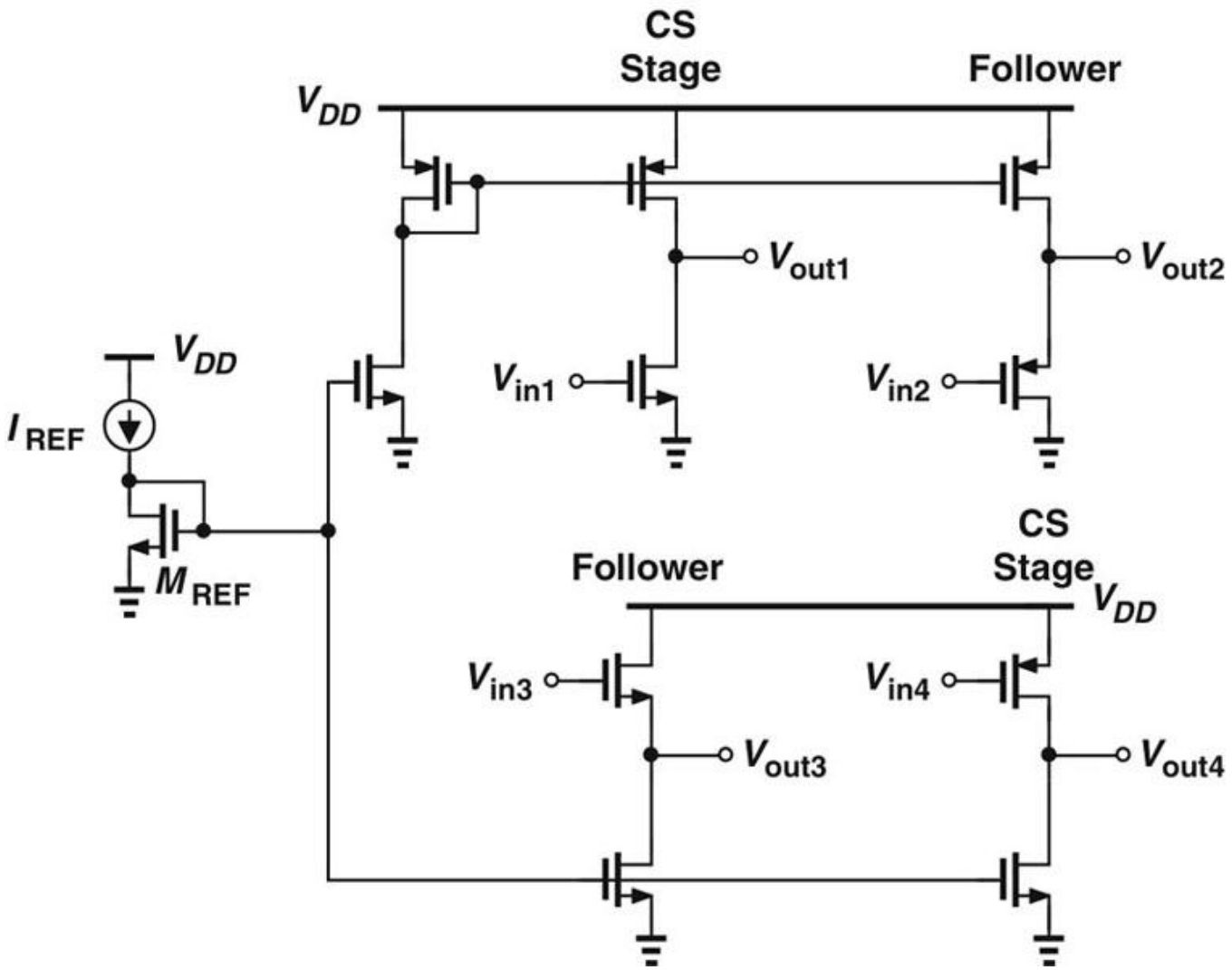
Channel-length modulation would lead to errors!!

Current Scaling

<Example 9.21> Design a current mirror that produces I_1 and I_2 from a 0.3mA reference.

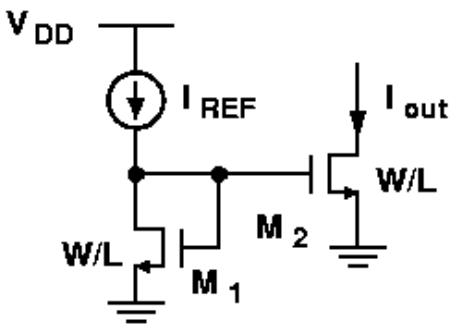


CMOS Current Mirror



Current Mirror with r_O

- Channel length modulation effect results in significant error in copying currents.

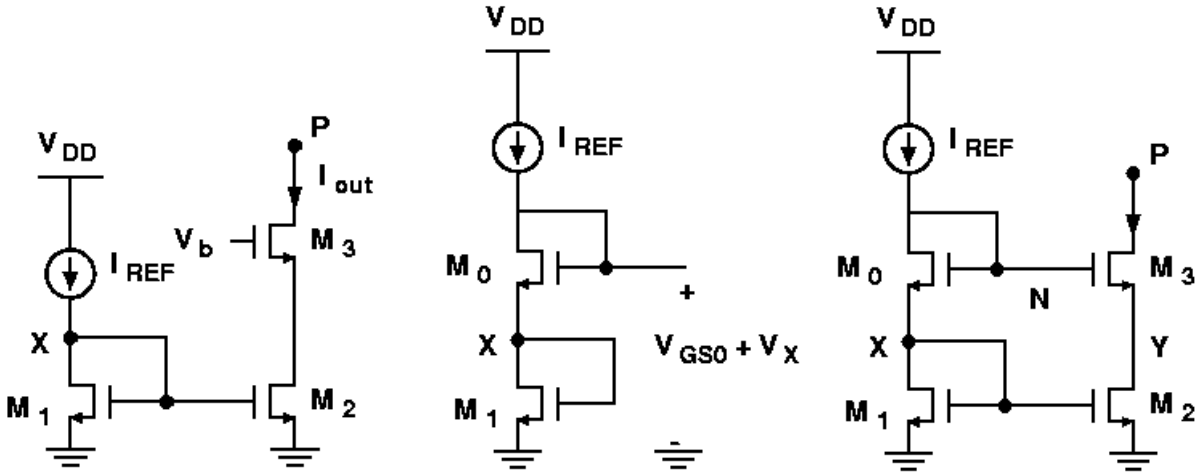


$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS1}), \quad I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS2})$$

- As $\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1}\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}}$, for $I_{D1} = I_{D2}$, V_{DS1} must be equal to V_{DS2}.

- Use cascode structure to improve the ratio accuracy of current mirror.

Cascode Current Mirror



- V_b is chosen such that $V_Y = V_X$.

$$V_b - V_{GS3} = V_X, \quad V_b = V_{GS3} + V_X, \quad V_N = V_{GS0} + V_X$$

$$\text{if} \quad \frac{(W/L)_3}{(W/L)_0} = \frac{(W/L)_2}{(W/L)_1}, \quad \text{then} \quad V_{GS0} = V_{GS3} \quad \text{and} \quad V_X = V_Y$$

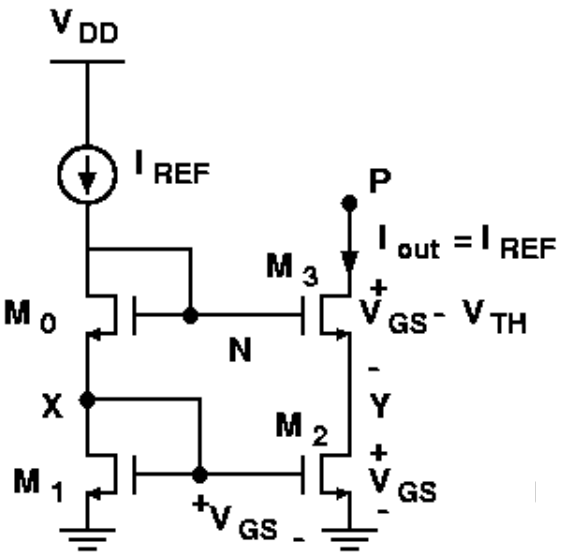
- Such accuracy is obtained at the cost of the voltage headroom consumed by M_3.

Cascode Current Mirror

- The minimum allowable voltage at node P is equal to

$$V_N - V_{TH} = V_{GS1} + V_{GS0} - V_{TH}$$
$$= (V_{GS1} - V_{TH}) + (V_{GS0} - V_{TH}) + V_{TH}$$

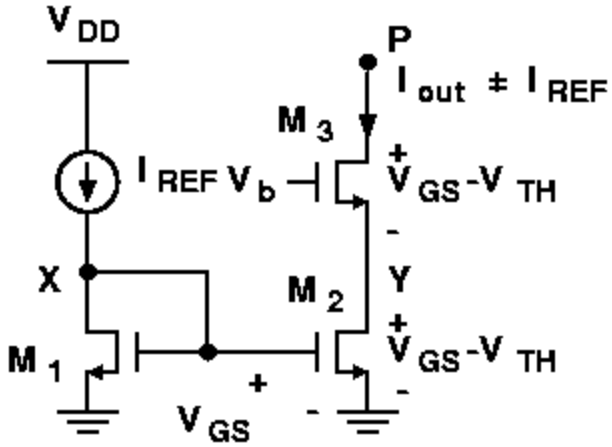
- The voltage of $V_N = V_{GS1} + V_{GS0}$



- For M_2 to be in saturation region, V_b can be chosen as low as

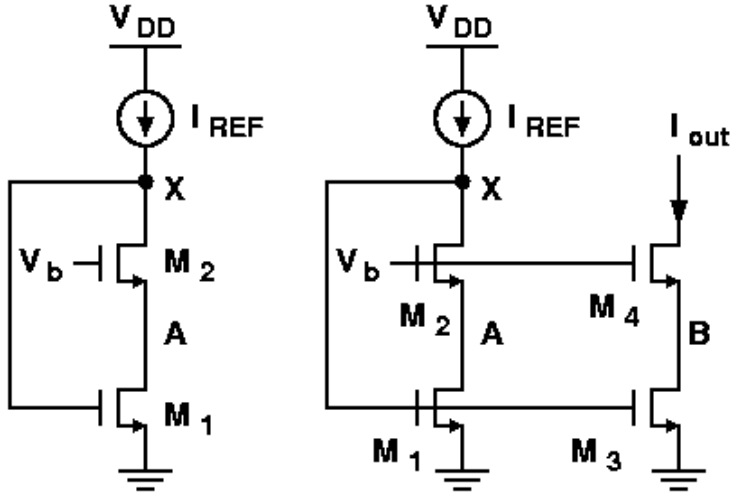
$$V_b = V_{GS3} + V_{DS2}$$

- But the output current does not accurately track I_{REF}.



Wide-Swing Cascode Current Mirror

- To eliminate the accuracy-headroom trade-off.



- For M2 to be saturated

$$V_b - V_{TH2} \le V_X (= V_{GS1})$$

- For M1 to be saturated

$$V_{GS1} - V_{TH1} \le V_A (= V_b - V_{GS2})$$

- Thus

$$V_{GS2} + (V_{GS1} - V_{TH1}) \le V_b \le V_{GS1} + V_{TH2}$$

- A solution exist if

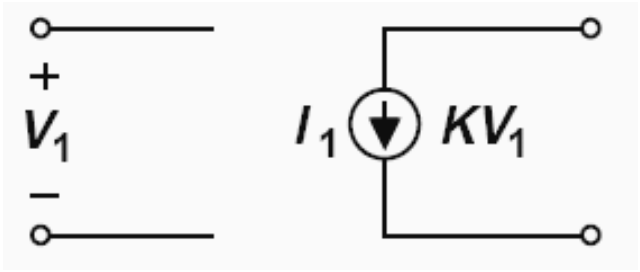
$$V_{GS2} + (V_{GS1} - V_{TH1}) \le V_{GS1} + V_{TH2} \Rightarrow V_{GS2} - V_{TH2} \le V_{TH1}$$

- Let

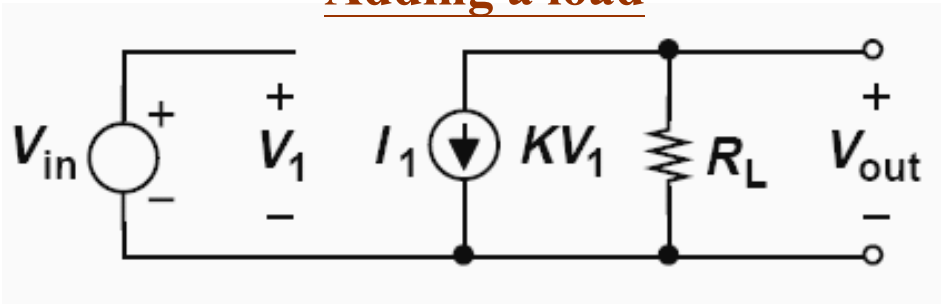
$$V_{GS2} = V_{GS4} \Rightarrow V_b = V_{GS2} + (V_{GS1} - V_{TH1}) = V_{GS4} + (V_{GS3} - V_{TH3})$$

Voltage-Dependent Current Source

Voltage-dependent current source



Adding a load



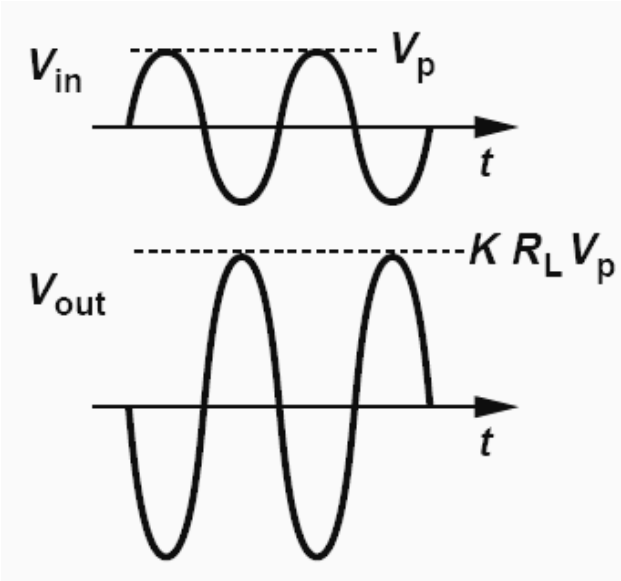
Simple amplifier

$$V_1 = V_{in}$$

$$V_{out} = -R_L I_1$$

$$V_{out} = -KR_L V_{in}.$$

$$A_V = \frac{V_{out}}{V_{in}} = -KR_L,$$



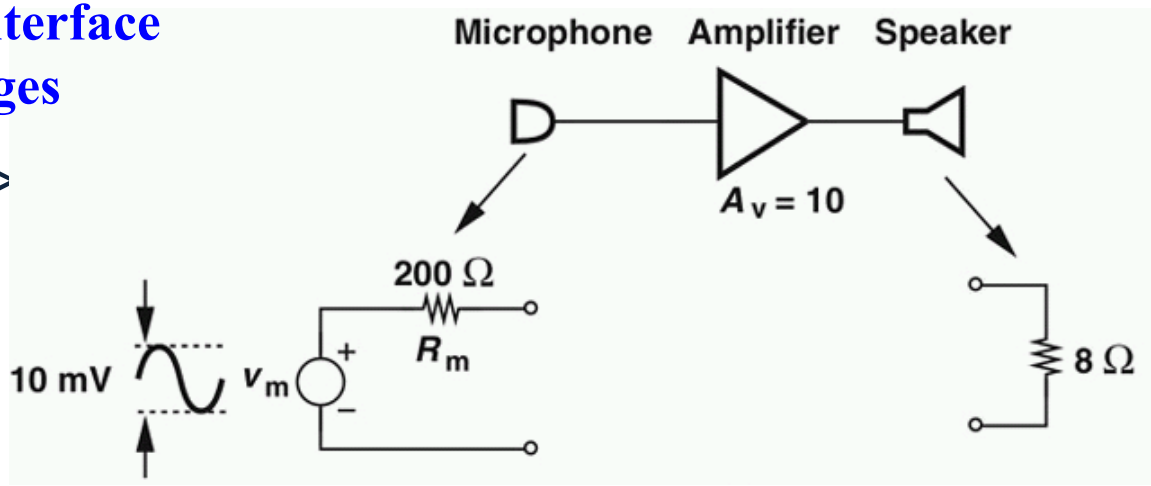
- <More aspects>
- Power dissipation
- Speed
- Noise

A voltage-dependent current source can provide signal amplification

Input and Output Impedances

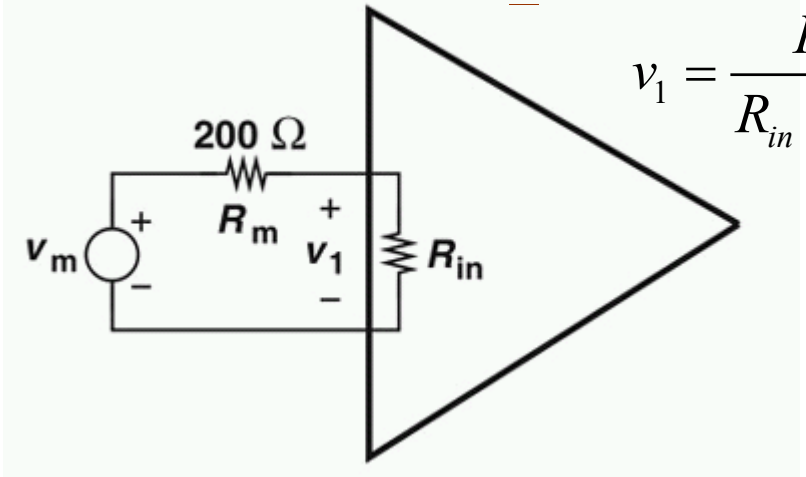
Critical role in its capability to interface with preceding and following stages

- <Ideal voltage amplifier>
- Input impedance = ∞
- Output impedance = 0



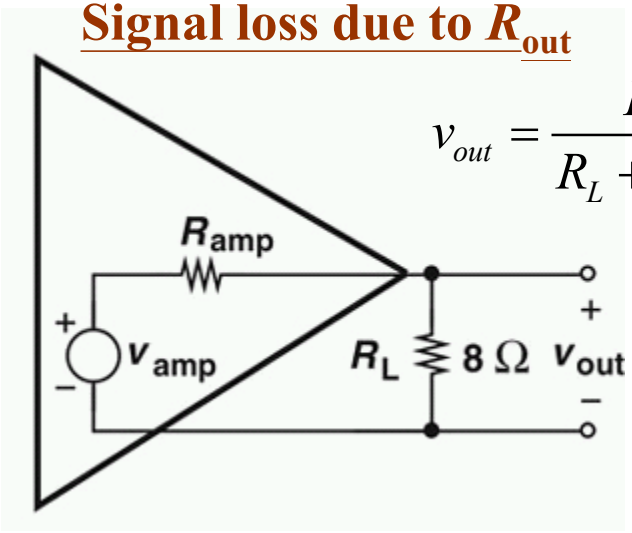
<Example 5.1>

Signal loss due to R_{in}



$$v_1 = \frac{R_{in}}{R_{in} + R_m} v_m .$$

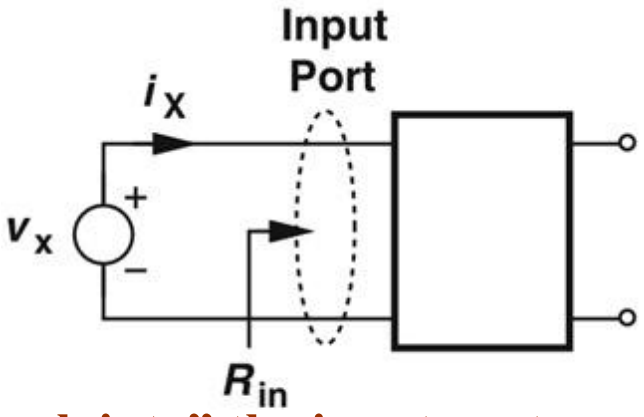
Signal loss due to R_{out}



$$v_{out} = \frac{R_L}{R_L + R_{amp}} v_{amp} .$$

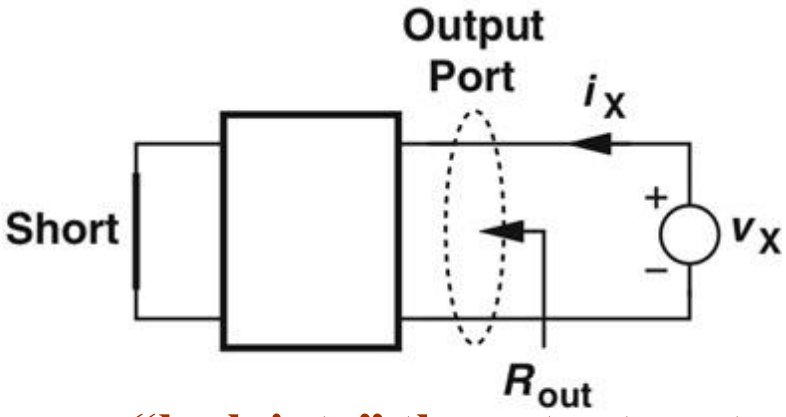
How to Measure Rin and Rout?

- For two-terminal devices
- All independent sources in the circuit are set to zero
  - Voltage source: short
  - Current source: open
- Apply a voltage source to the two nodes (ports) of interest
- Measure the resulting current
- Impedance = v_X/i_X



"look into" the input port

(a)

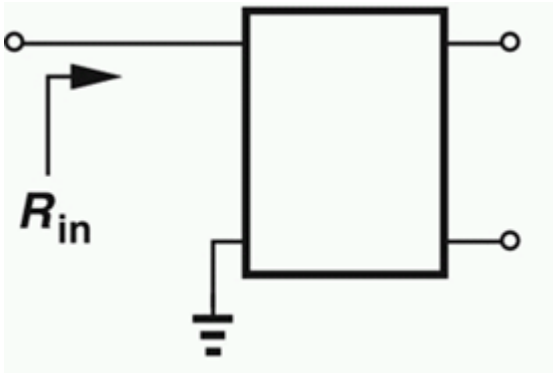


"look into" the output port

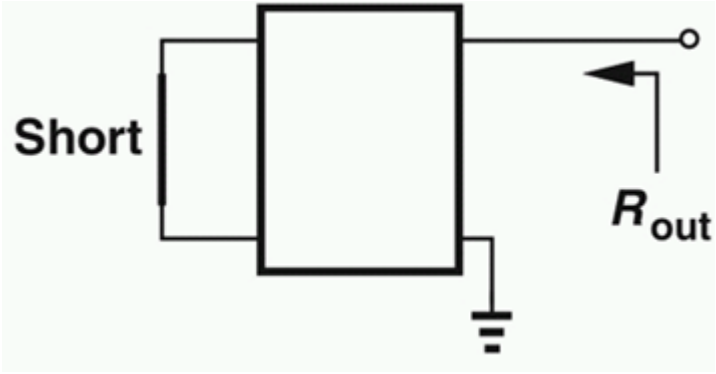
(b)

Biasing

Impedance seen at a node (assuming the other node is ground)

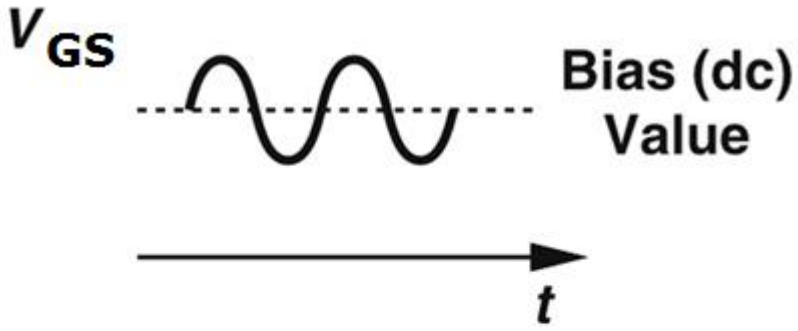


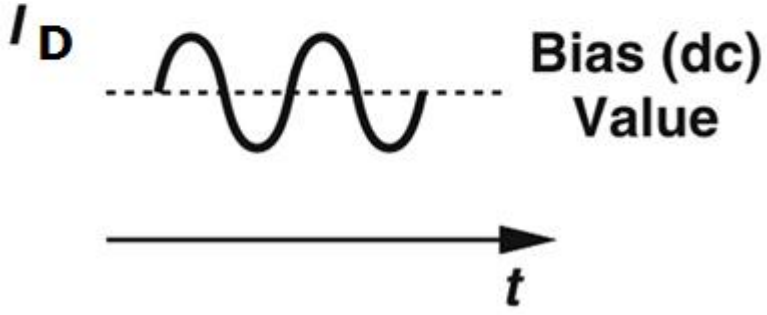
"look into" the input node



"look into" the output node

Transistors and circuits must be biased because (1) transistors must operate in the active region, (2) their small-signal parameters depend on the bias conditions.





Procedure for Analysis

Superposition principle:

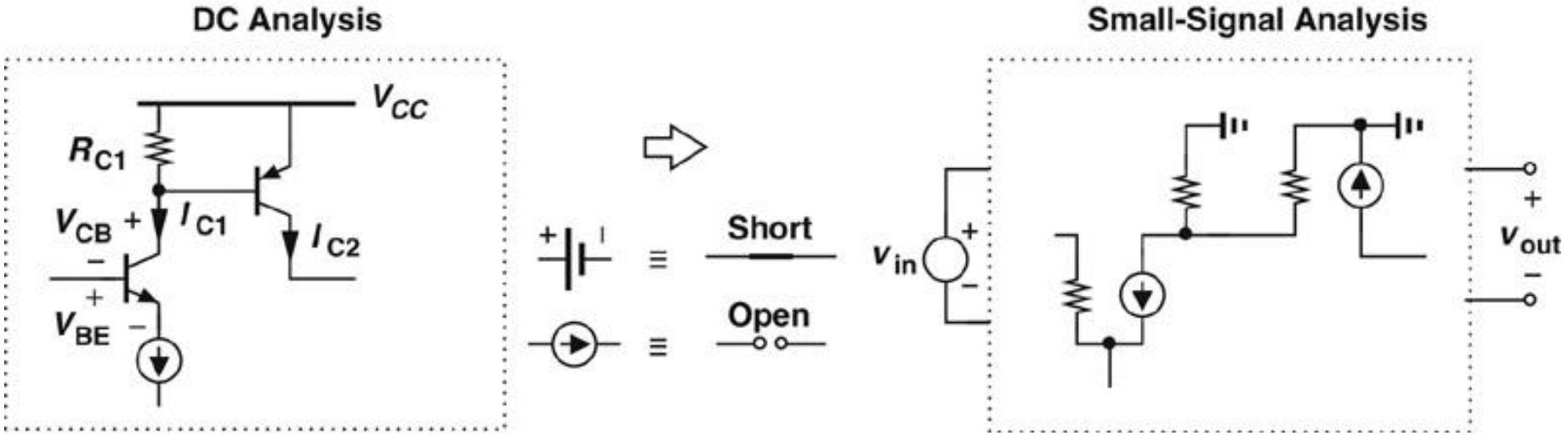
(1) DC analysis (Bias analysis): Compute the operating (quiescent) conditions (terminal voltages and currents) of each transistor *in the absence of signals*

a. **Determine the region of operation (active or saturation)**

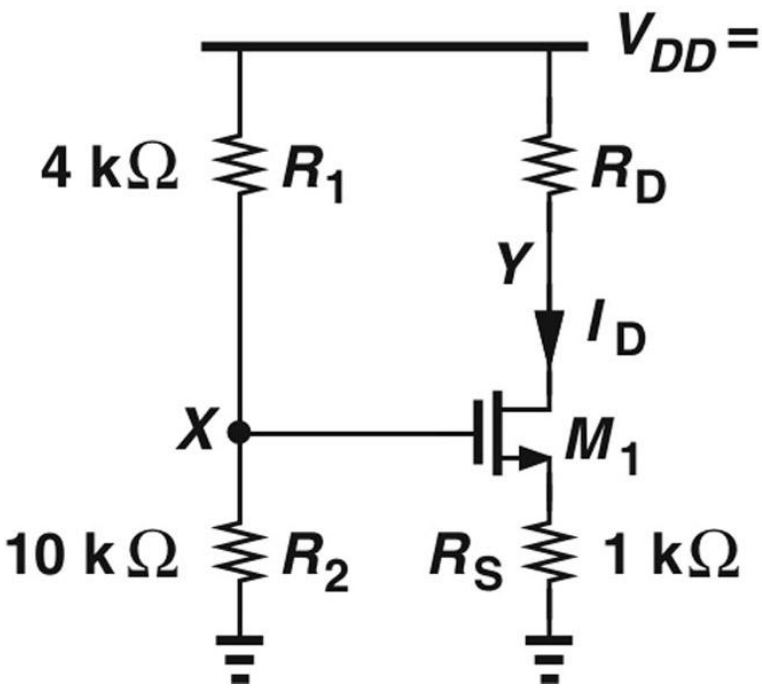
b. **Determine the small-signal parameters of each device**

(2) Small-signal analysis: Study the response of the circuit to small signals and compute quantities (A_v, R_{in}, R_{out}) *in the absence of sources*

Rule of thumb: 10% variation in the collector current as the upper bond



MOS Stage with Biasing



$$V_X = \frac{R_2}{R_1 + R_2} V_{DD}. \qquad V_X = V_{GS} + I_D R_S$$

$$\frac{R_2}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S.$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2.$$

Find I_D, V_{GS}

Iteration

$$\left(\frac{R_2}{R_1 + R_2} V_{DD} - V_{GS} \right) \frac{1}{R_S} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2.$$

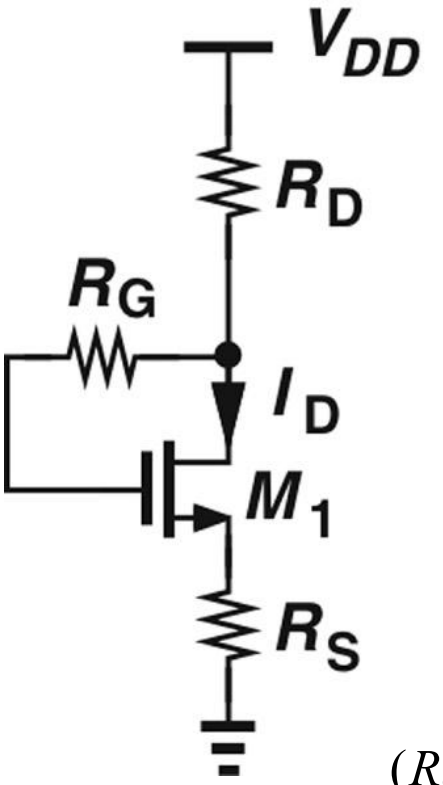
$$V_{GS} = -(V_1 - V_{TH}) + \sqrt{(V_1 - V_{TH})^2 - V_{TH}^2 + \frac{2R_2}{R_1 + R_2} V_1 V_{DD}}, = -(V_1 - V_{TH}) + \sqrt{V_1^2 + 2V_1 \left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH} \right)},$$

$$V_1 = \frac{1}{\mu_n C_{ox} \frac{W}{L} R_S}.$$

$V_Y \geq V_X - V_{TH}$ to ensure saturation

Self-Biased MOS Stage

The circuit



- <Observations>
- M1 is in saturation
- VRG = 0

$$I_D R_D + V_{GS} + R_S I_D = V_{DD}.$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[V_{DD} - (R_S + R_D)I_D - V_{TH}]^2,$$

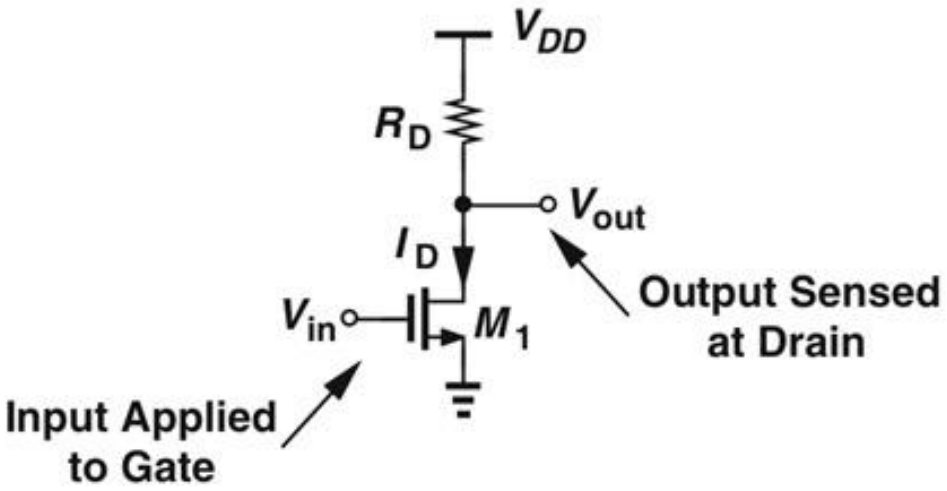
$$(R_S + R_D)^2 I_D^2 - 2\left[(V_{DD} - V_{TH})(R_S + R_D) + \frac{1}{\mu_n C_{ox}\dfrac{W}{L}}\right] I_D + (V_{DD} - V_{TH})^2 = 0.$$

Elementary Gain Stages

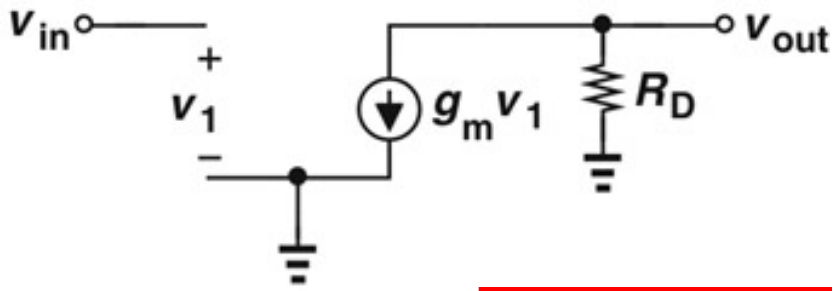
- Current Source and Biasing
- CMOS Amplifiers (CS, CG, CD, Cascode)
- Differential Amplifiers

Common-Source Stage

The circuit



Small-signal model



$$v_{in} = v_1$$

$$v_{out} = -g_m v_1 R_D$$

$$\frac{v_{out}}{v_{in}} = -g_m R_D,$$

Discussion

$$g_m = \sqrt{2\mu_n C_{ox}(W/L) I_D}$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D R_D},$$

For M_1 to remain in saturation:

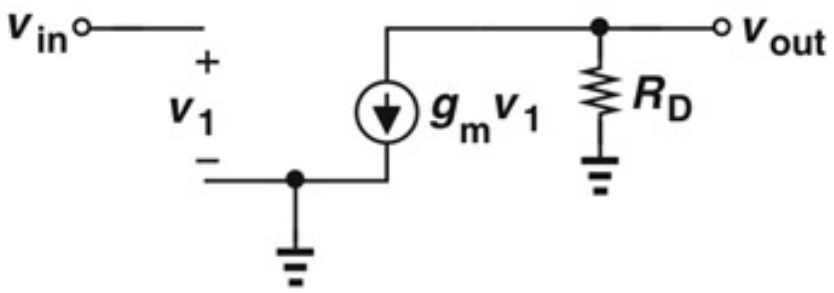
$$V_{DD} - R_D I_D > V_{GS} - V_{TH},$$

$$R_D I_D < V_{DD} - (V_{GS} - V_{TH}).$$

Voltage gain limited by V_{DD}!!

Input and Output Impedances

Small-signal model

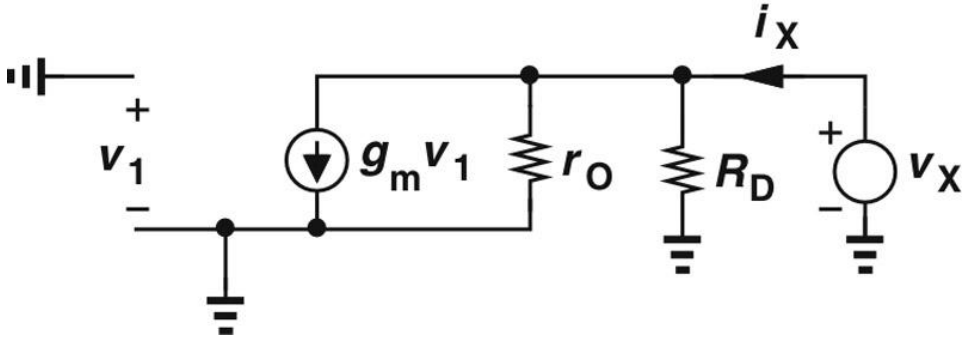


$$R_{in} = \infty, \qquad \boldsymbol{R_{in} = r_\pi \text{ for bipolar}}$$

$$R_{out} = R_D .$$

$$A_v = -g_m R_D$$

Channel-length modulation included



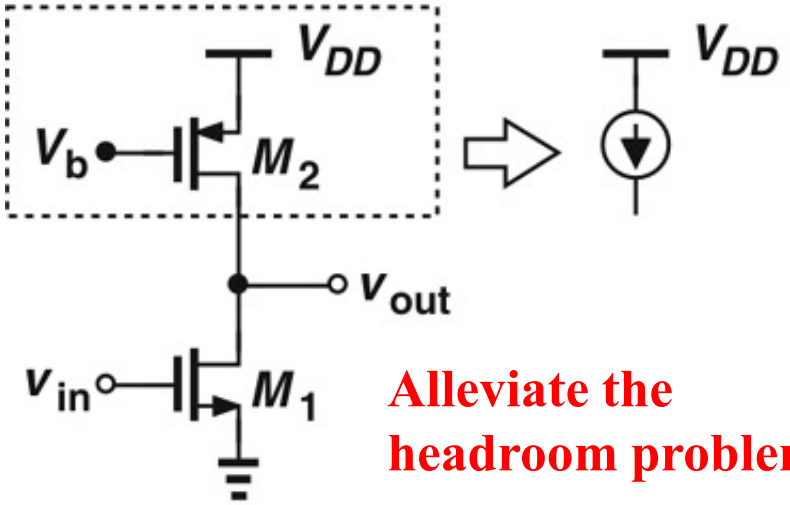
$$A_v = -g_m \left(R_L \parallel r_O \right)$$

$$R_{in} = \infty$$

$$R_{out} = R_L \parallel r_O$$

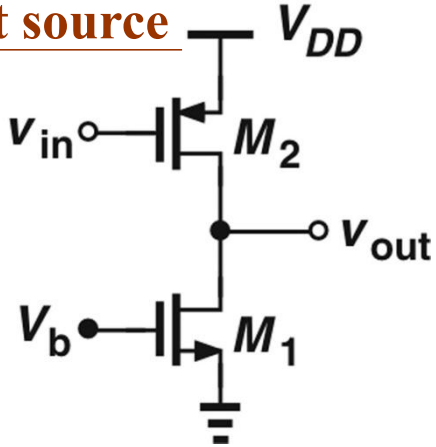
CS Stage with Current-Source Load

Use PMOS as current source

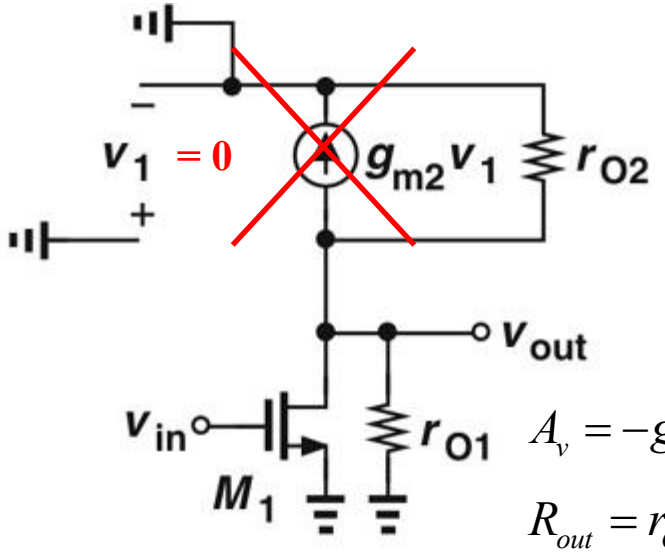


Alleviate the headroom problem

Use NMOS as current source with PMOS CS Stage



Small-signal model



$$v_1 = 0$$

$$g_{m2}v_1 = 0$$

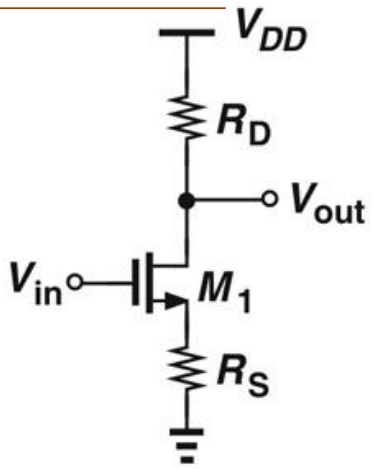
$$A_v = -g_{m1}(r_{O1} \| r_{O2})$$

$$R_{out} = r_{O1} \| r_{O2}.$$

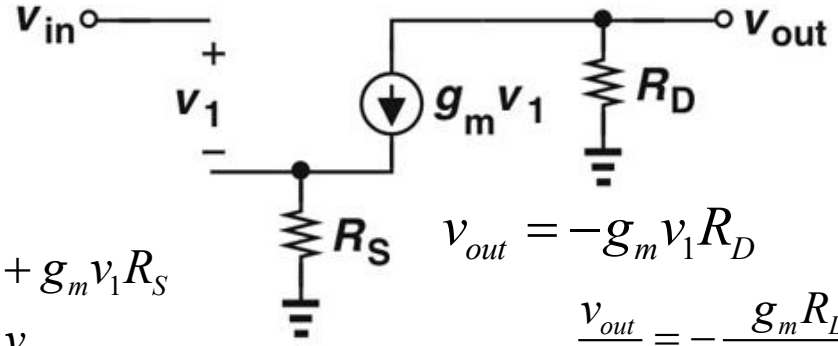
$$A_v = -g_{m2}(r_{O1} \| r_{O2}).$$

CS Stage with Degeneration

The circuit



Small-signal model



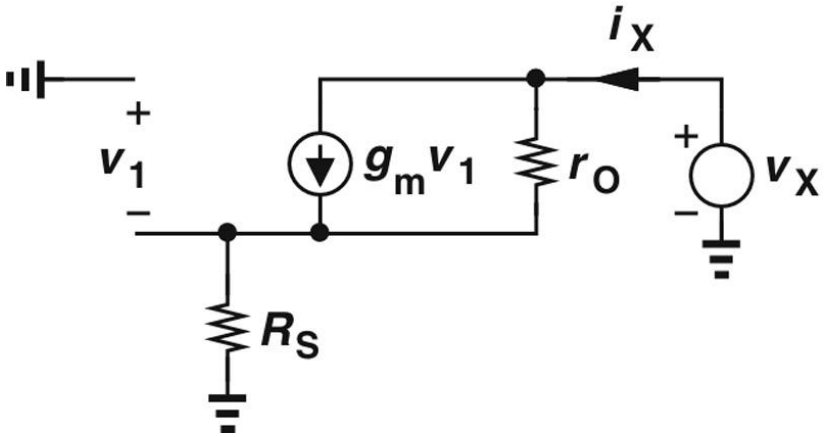
$$v_{in} = v_1 + g_m v_1 R_S$$

$$v_1 = \frac{v_{in}}{1 + g_m R_S}.$$

$$v_{out} = -g_m v_1 R_D$$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_D}{1 + g_m R_S} = -\frac{R_D}{\frac{1}{g_m} + R_S},$$

Output impedance



$$v_1 = -i_X R_S$$

$$i_X - g_m v_1 = i_X - g_m(-i_X R_S) = i_X + g_m i_X R_S$$

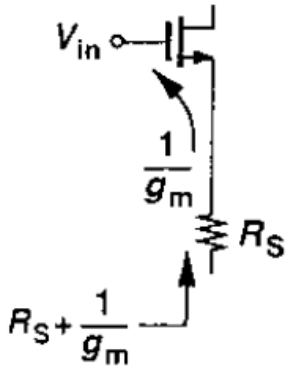
$$r_O(i_X + g_m i_X R_S) + i_X R_S = v_X,$$

$$\frac{v_X}{i_X} = r_O(1 + g_m R_S) + R_S$$

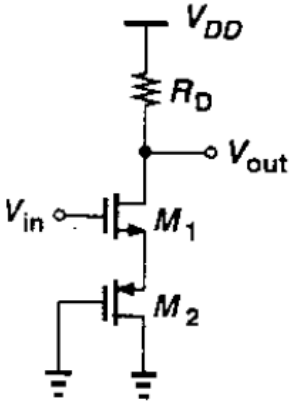
$$= (1 + g_m r_O)R_S + r_O \approx g_m r_O R_S + r_O.$$

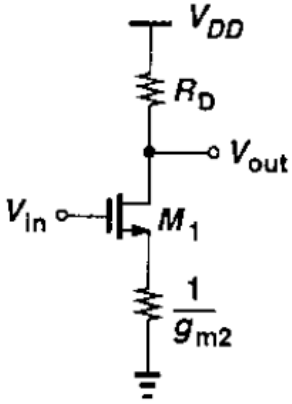
Formulate Gain by Inspection

- Magnitude of gain as the resistance seen at the drain node divided by the total resistance in the source path



$$A_v = -\frac{R_D}{1/g_m + R_S}$$

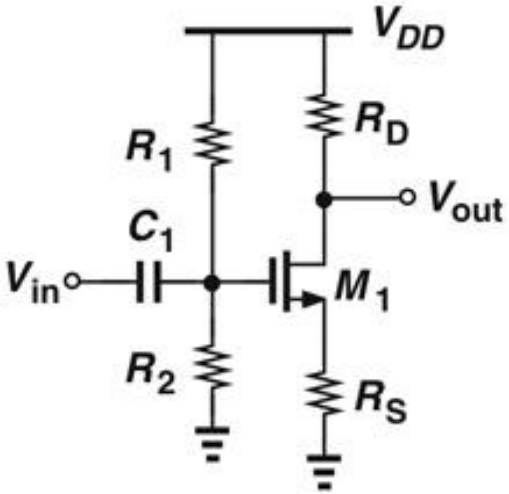




$$A_v = -\frac{R_D}{1/g_{m1} + 1/g_{m2}}$$

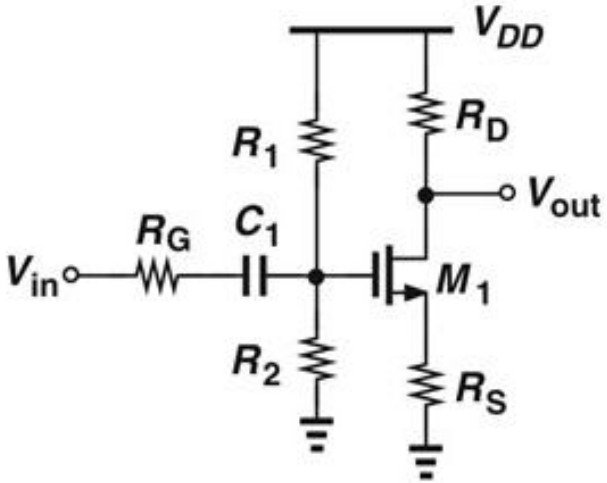
CS Core with Biasing

CS with biasing



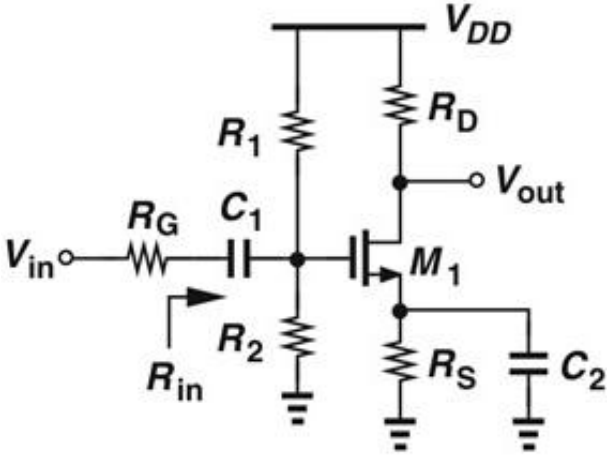
$$R_{in} = R_1 \parallel R_2.$$

With signal source resistance



$$A_v = \frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S},$$

With bypass capacitor



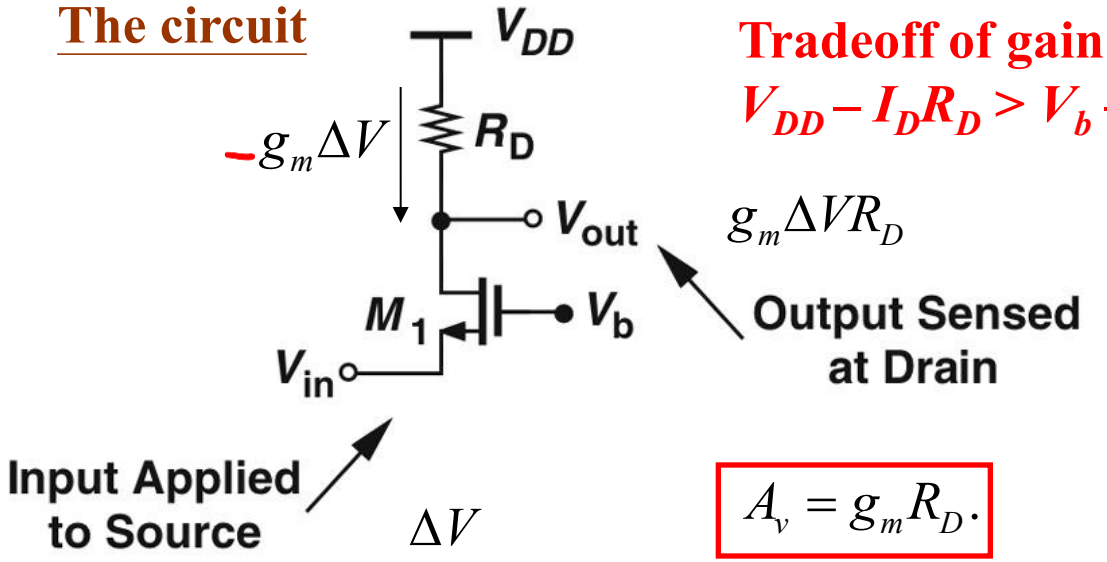
$$R_{in} = R_1 \parallel R_2,$$

$$A_v = -\frac{R_1 \parallel R_2}{R_G + R_1 \parallel R_2} g_m R_D.$$

- **Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.**

Common-Gate Stage

The circuit



Tradeoff of gain and headroom!

$V_{DD} - I_D R_D > V_b - V_{TH}$ for M_1 stays in saturation

$$A_v = g_m R_D.$$

<Example 7.12> A microphone with dc level of zero drives a CG stage biased at I_D = 0.5mA. If W/L = 50, $\mu_n C_{ox}$ = 100 μA/V², V_{TH} = 0.5V, and V_{DD} = 1.8V, determine the maximum allowable value of R_D and hence the maximum voltage gain. Neglect channel-length modulation.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

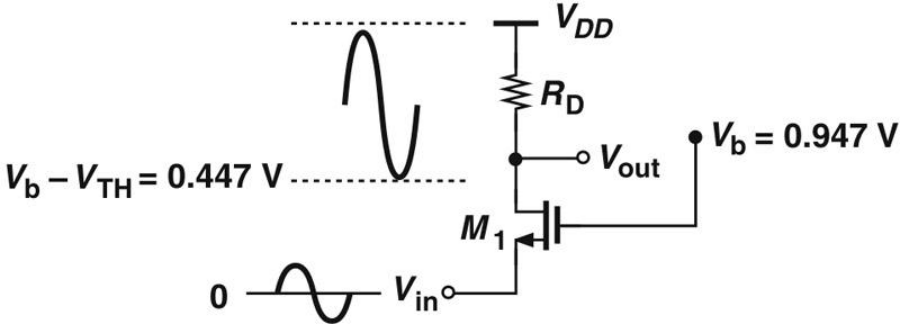
$$\Rightarrow V_{GS} = 0.947\text{V}.$$

$$V_{DD} - I_D R_D > V_b - V_{TH}$$

$$\Rightarrow R_D < 2.71\text{k}\Omega.$$

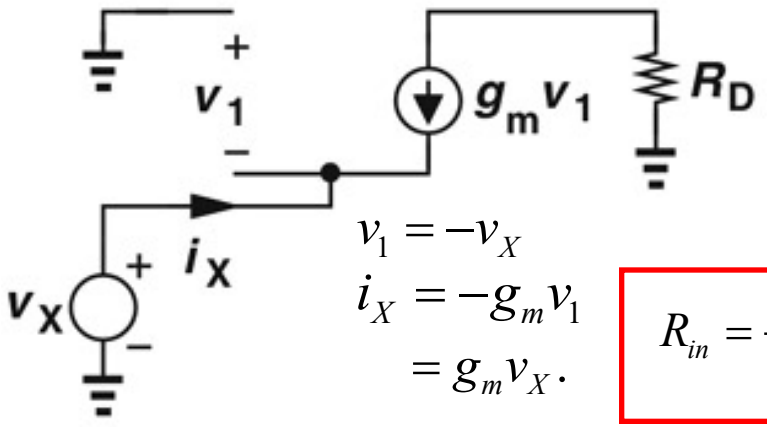
$$\Rightarrow g_m = (447\Omega)^{-1}$$

$$\Rightarrow A_v \le 6.06.$$



Input and Output Impedances

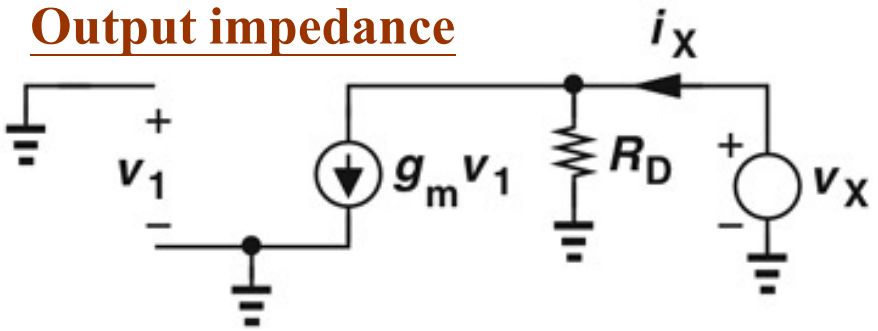
Input impedance



$$v_1 = -v_X$$
$$i_X = -g_m v_1$$
$$= g_m v_X .$$

$$R_{in} = \frac{1}{g_m},$$

Output impedance

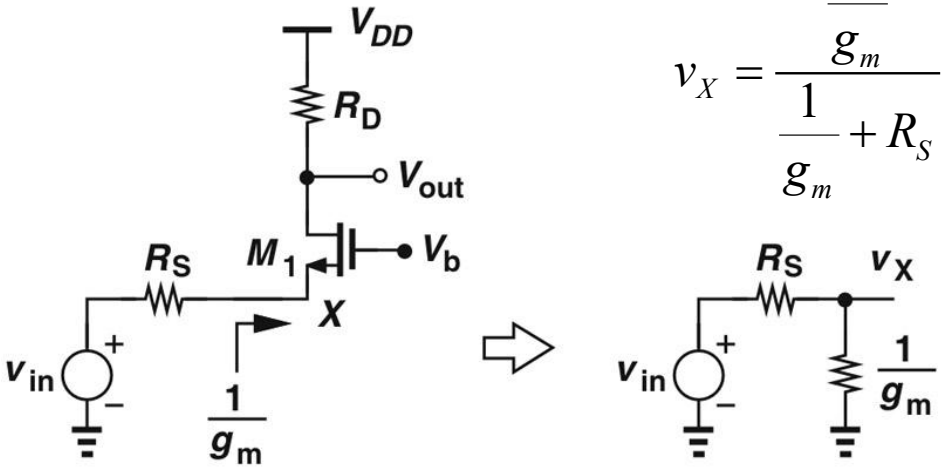


$$v_1 = 0$$

$$R_{out} = R_D,$$

$$A_I = \frac{i_d}{i_s} = 1$$

With source impedance

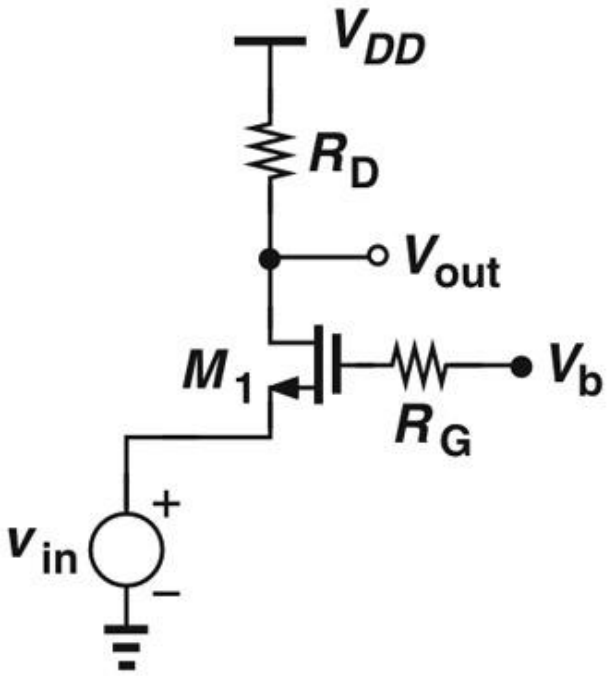


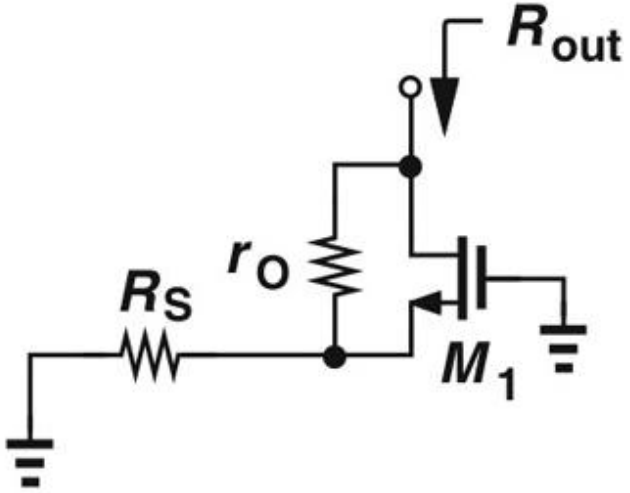
$$v_X = \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} v_{in} = \frac{1}{1 + g_m R_S} v_{in}.$$

$$\frac{v_{out}}{v_{in}} = \frac{v_{out}}{v_X} \cdot \frac{v_X}{v_{in}}$$
$$= \frac{g_m R_D}{1 + g_m R_S}$$
$$= \frac{R_D}{\frac{1}{g_m} + R_S}.$$

Same as degenerated CS!!

Generalized CG Behavior

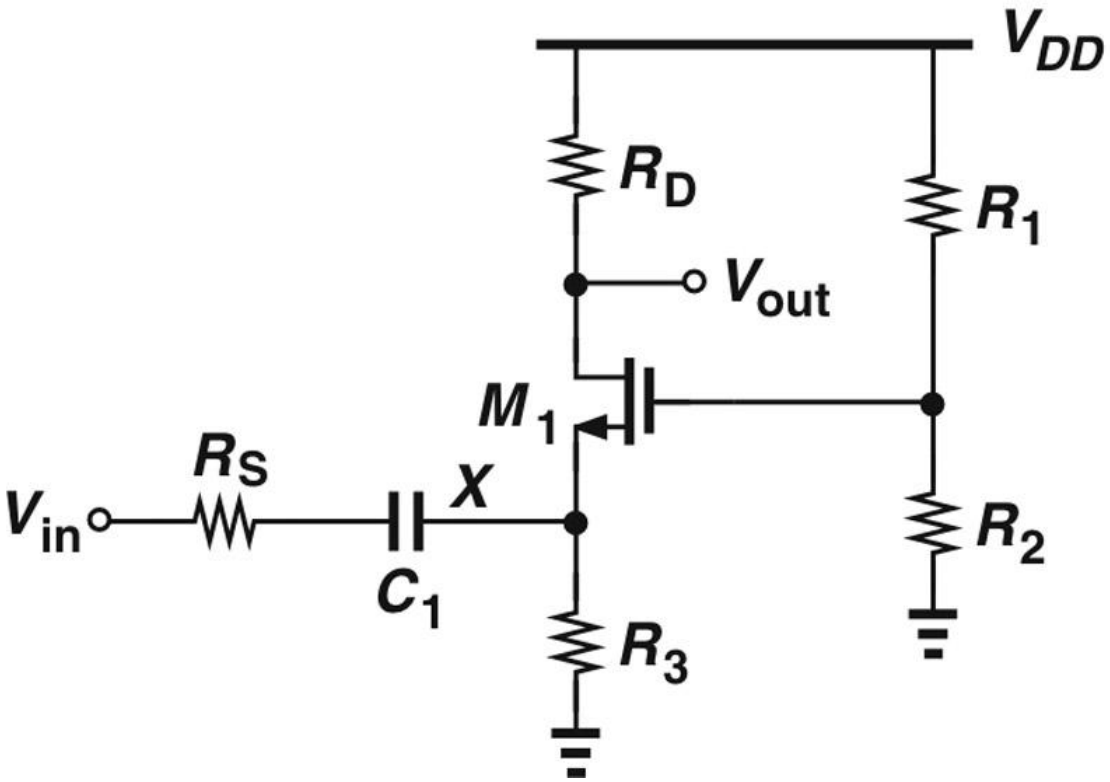




$$R_{out} = (1 + g_m r_O) R_S + r_O$$

- **When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it (at low frequencies).**
- **The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.**

CG Stage with Biasing



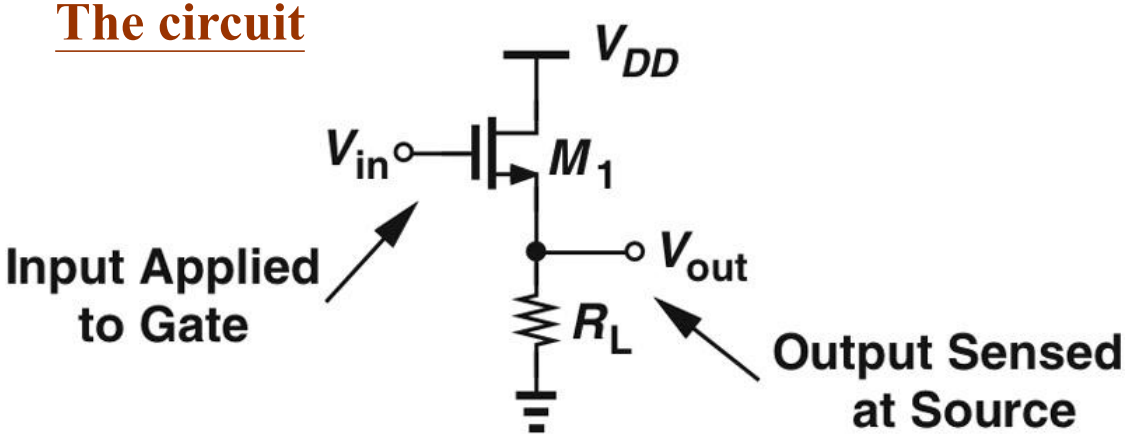
$$\frac{v_{out}}{v_{in}} = \frac{v_X}{v_{in}} \cdot \frac{v_{out}}{v_X}$$

$$= \frac{R_3 \,||\, (1/g_m)}{R_3 \,||\, (1/g_m) + R_S} \cdot g_m R_D,$$

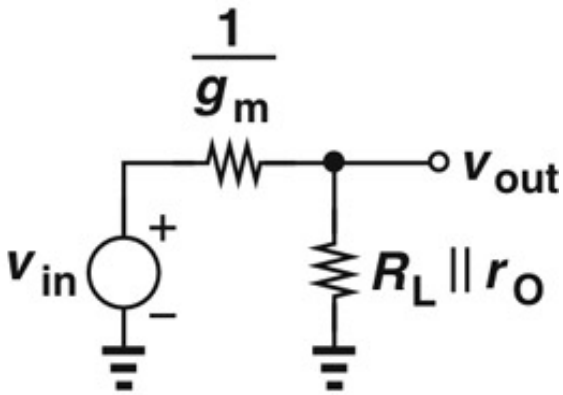
- **R_1 and R_2 provide gate bias voltage, and R_3 provides a path for DC bias current of M_1 to flow to ground.**

CD Stage: Source Follower

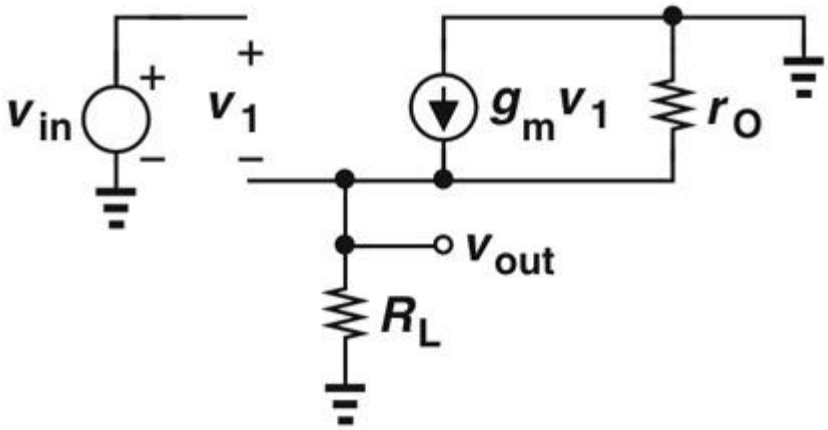
The circuit



Simplified circuit



Source follower core



$$g_m v_1 (r_O \| R_L) = v_{out}.$$

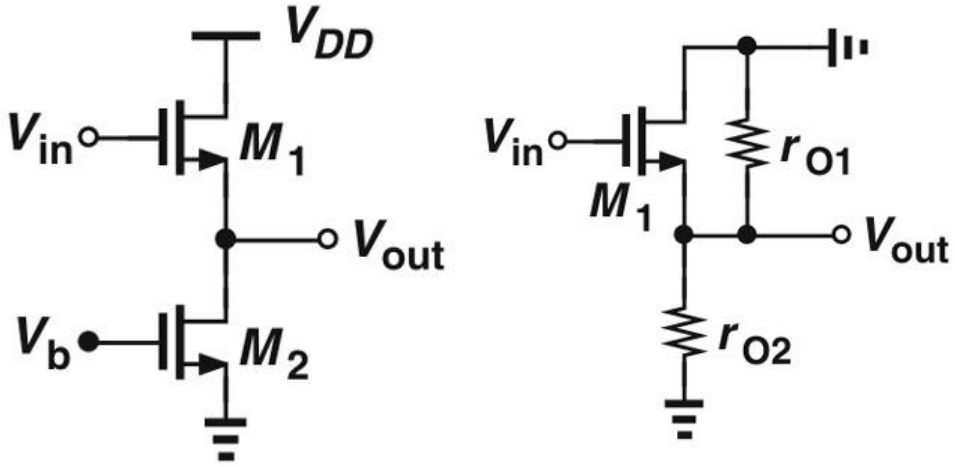
$$v_{in} = v_1 + v_{out}.$$

$$\frac{v_{out}}{v_{in}} = \frac{g_m (r_O \| R_L)}{1 + g_m (r_O \| R_L)} = \frac{r_O \| R_L}{\frac{1}{g_m} + r_O \| R_L}.$$

$$A_v < 1$$

Two Examples

<Example 7.16> Calculate the voltage gain of the circuit

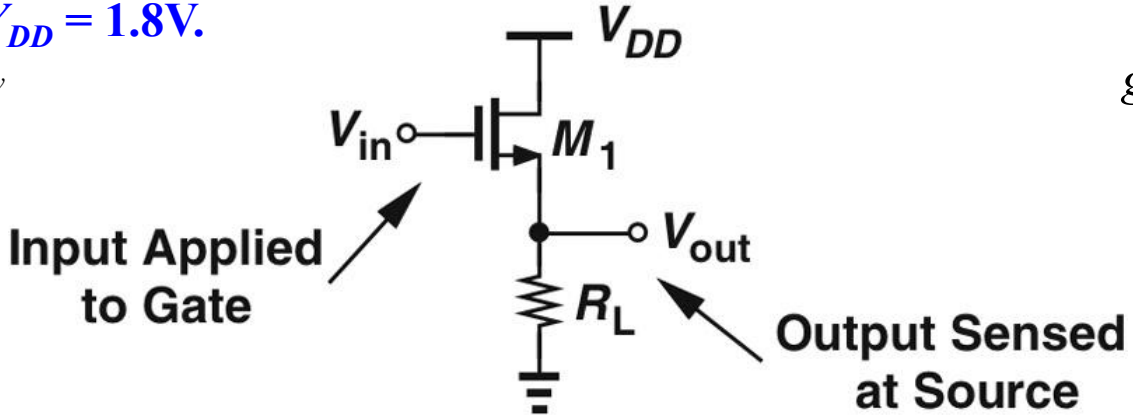


$$A_v = \frac{r_{O1} \| r_{O2}}{\frac{1}{g_{m1}} + r_{O1} \| r_{O2}}.$$

$$r_{o1} \| r_{o2} >> \frac{1}{g_{m1}}, A_v \approx 1$$

<Example 7.17> Design a source follower to drive a 50-Ω load with a voltage gain of 0.5 and a power budget of 10mW. Assume $\mu_n C_{ox}$ = 100 μA/V², V_{TH} = 0.5V, λ = 0, and V_{DD} = 1.8V.

A_v

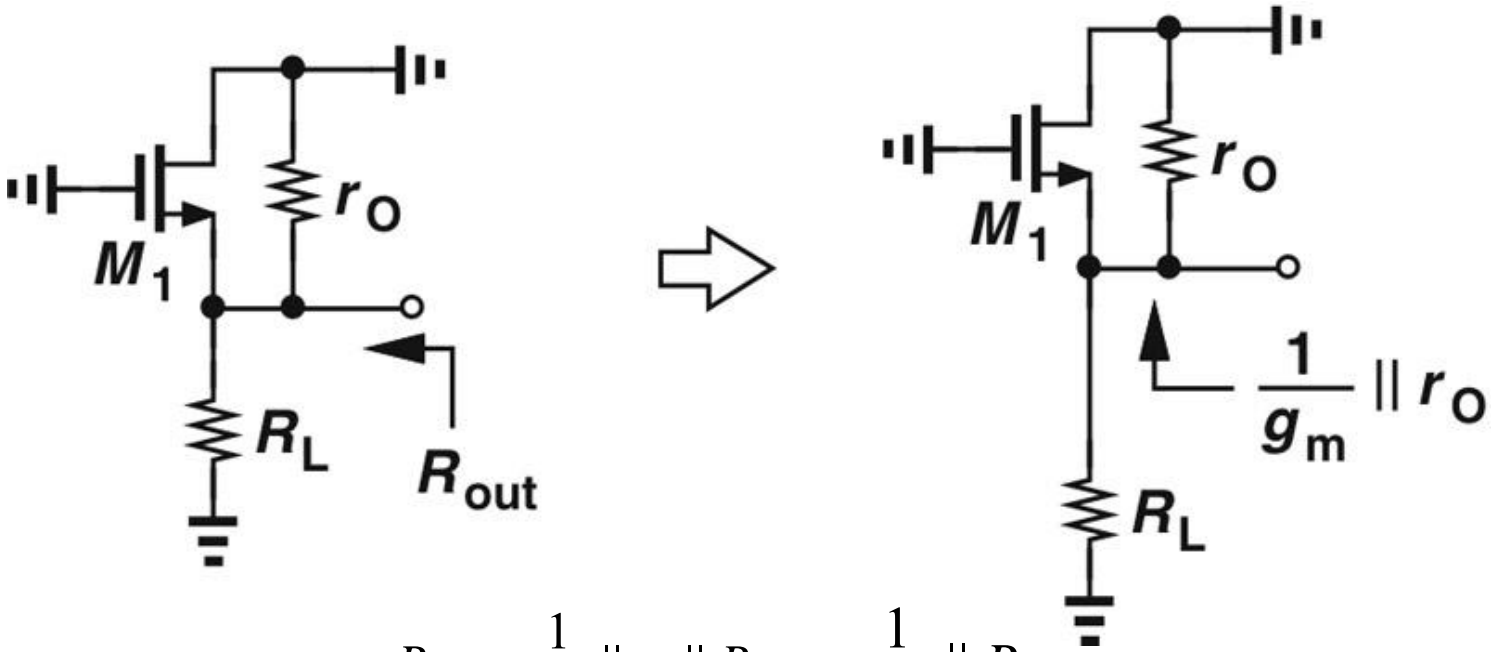


$$g_m = \frac{1}{50\Omega}. \qquad I_D = \frac{10mW}{1.8V} = 5.56mA$$

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$$

$$W/L = 360.$$

Output Resistance

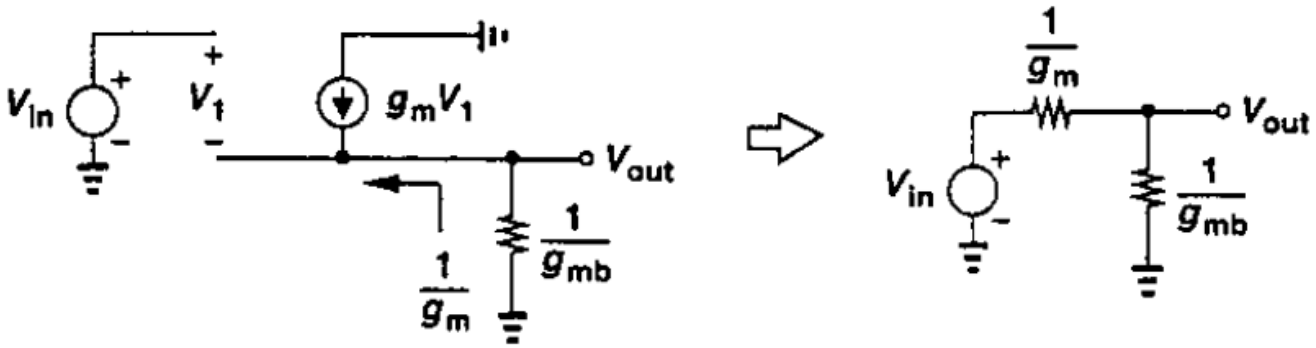


$$R_{out} = \frac{1}{g_m} \| r_O \| R_L \approx \frac{1}{g_m} \| R_L .$$

- **The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.**

Source Follower with Body Effect

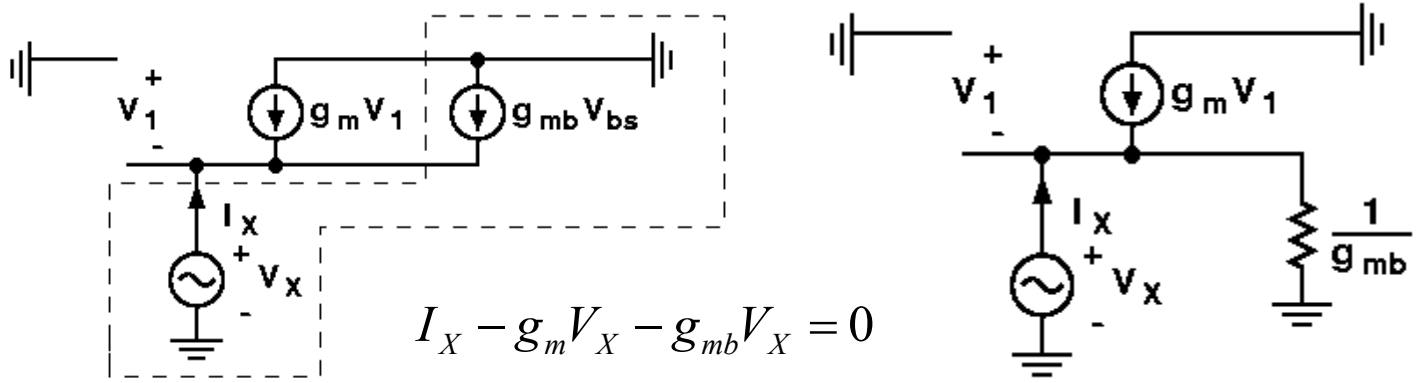
- Less-than-unity voltage gain of source follower with body effect
- $g_{mb} \approx 0.2\, g_m$, gain ≈ 1/1.2 ≈ 0.8 even with R_S = infinity



$$R_S = \infty$$

$$A_v = \frac{1/g_{mb}}{1/g_m + 1/g_{mb}} = \frac{g_m}{g_m + g_{mb}}$$

- Body effect decrease R_{out} of source follower

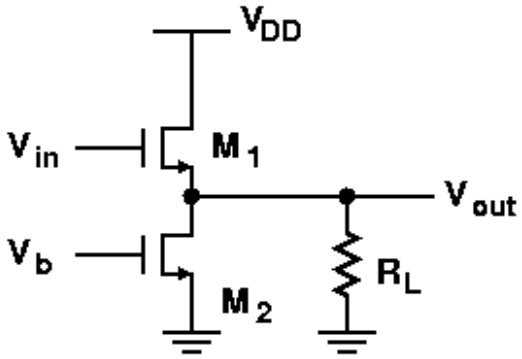


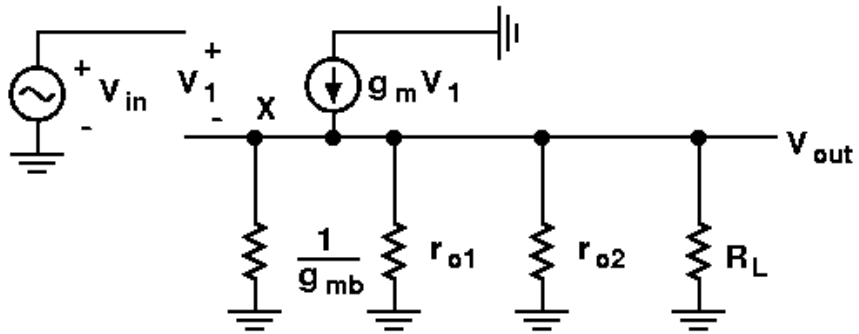
$$I_X - g_m V_X - g_{mb} V_X = 0$$

$$R_{out} = \frac{1}{g_m + g_{mb}}$$

Source Follower with r_o

- Source follower with finite channel-length modulation

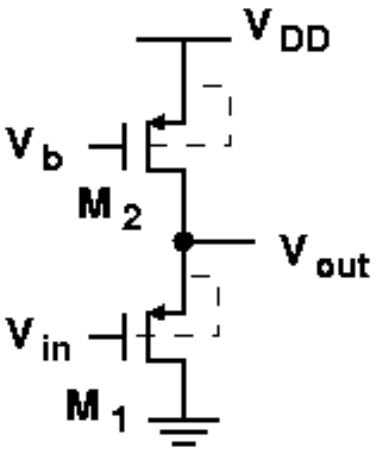


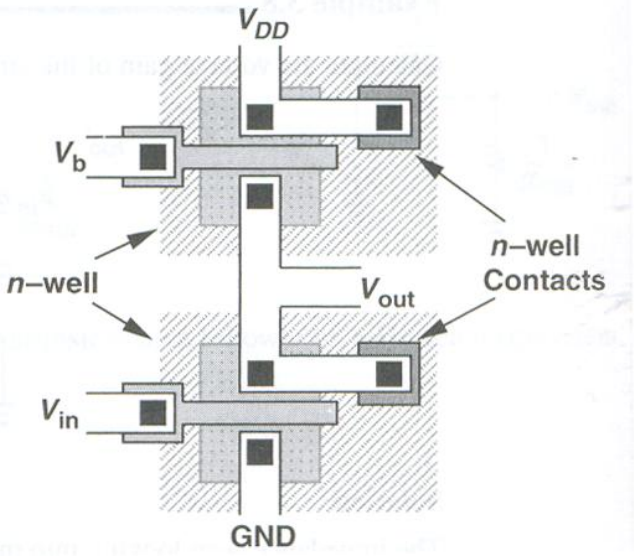


$$A_v = \frac{\frac{1}{g_{mb}} \| r_{O1} \| r_{O2} \| R_L}{\frac{1}{g_{mb}} \| r_{O1} \| r_{O2} \| R_L + \frac{1}{g_m}}$$

Source Follower Drawback

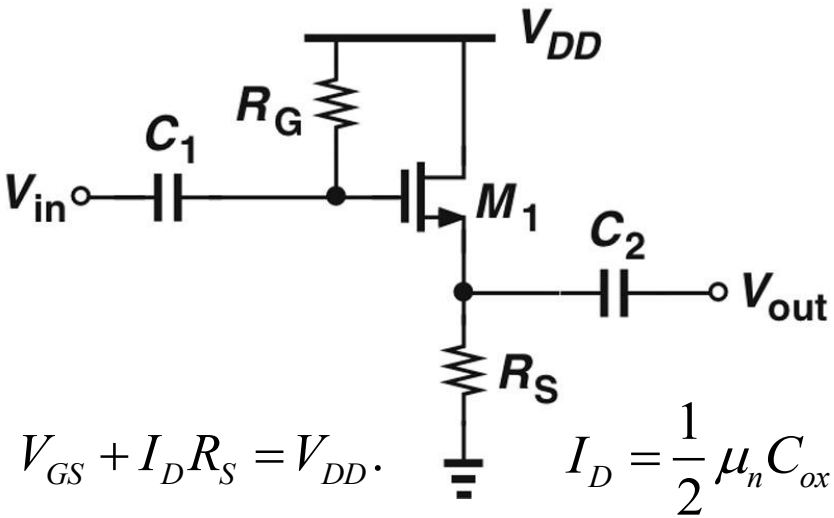
- Voltage headroom consumption due to level shift.
- Nonlinearity
  - Nonlinear dependence of V_{TH} upon the source potential.
  - r_O of the transistor also changes substantially with V_{DS}.
- PMOS source follower with no body effect





- Higher output impedance using PMOS source follower.

Source Follower with Biasing

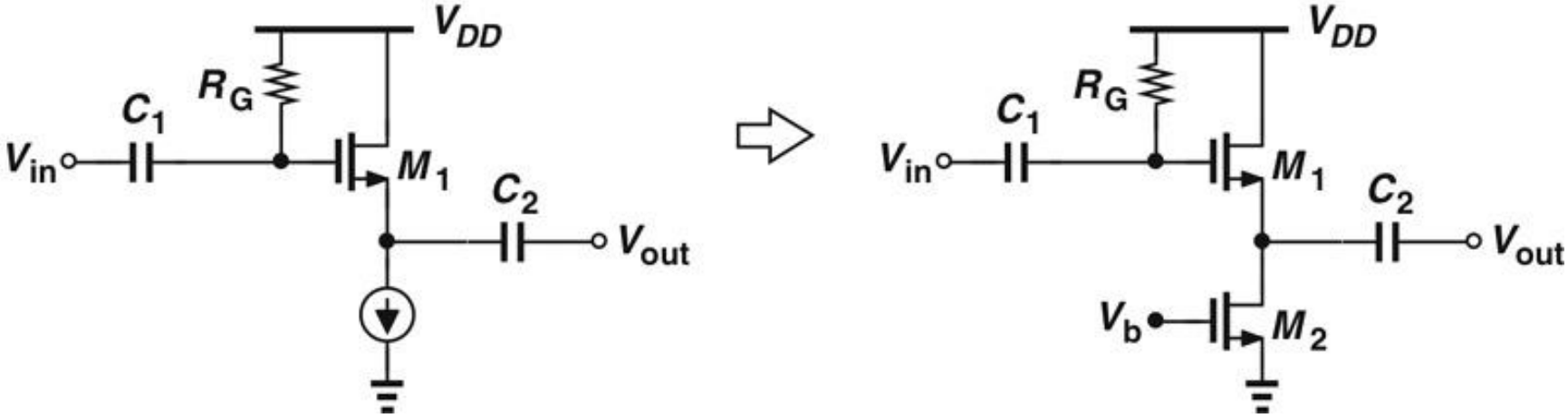


- Features:
- Input/output coupling capacitors
- RG establishes a dc voltage equal to VDD at the gate of M1
- RS sets the bias current
- M1 operates in saturation
- Input impedance = RG

$$V_{GS} + I_D R_S = V_{DD}. \qquad I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - I_D R_S - V_{TH})^2.$$

Bias current varies with supply voltage!

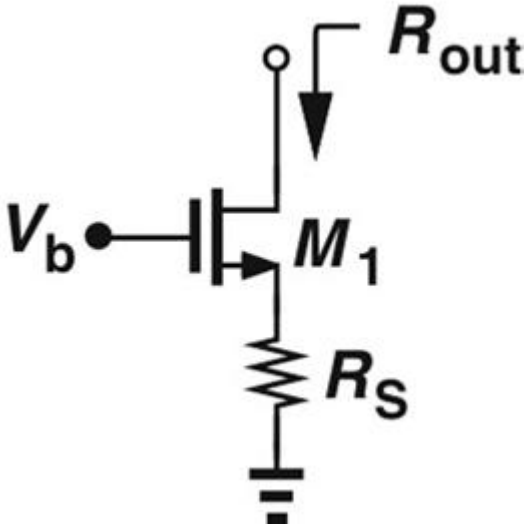
Supply-independent Biasing



Remember This?

Emitter (source) degeneration "boosts" the output impedance

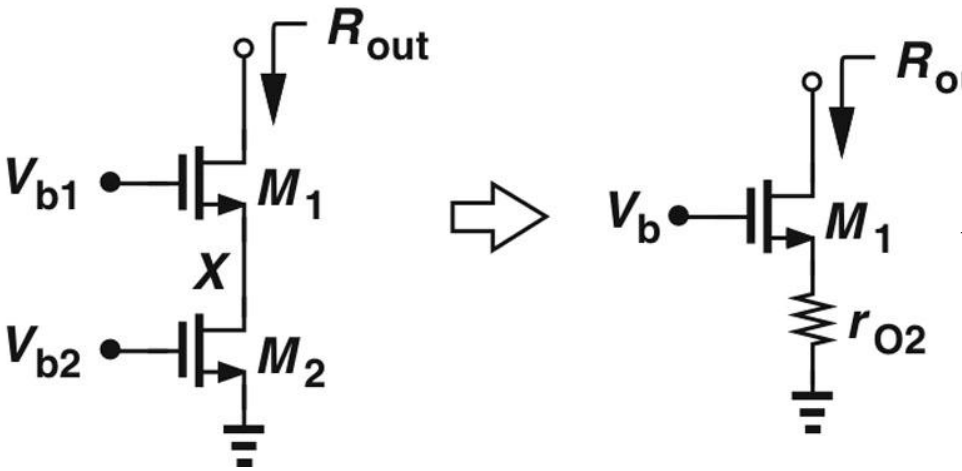
CS with source degeneration



$$R_{out2} = (1 + g_m R_S) r_O + R_S$$
$$= (1 + g_m r_O) R_S + r_O,$$

Voltage drop on degenerated resistor consumes headroom!!
How do we relax this problem??

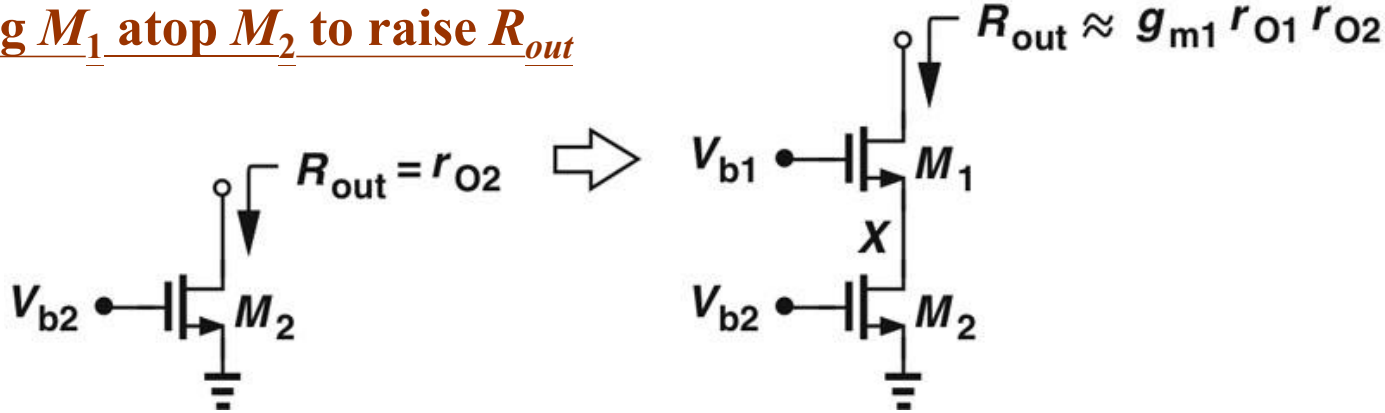
MOSFET Cascode Current Source



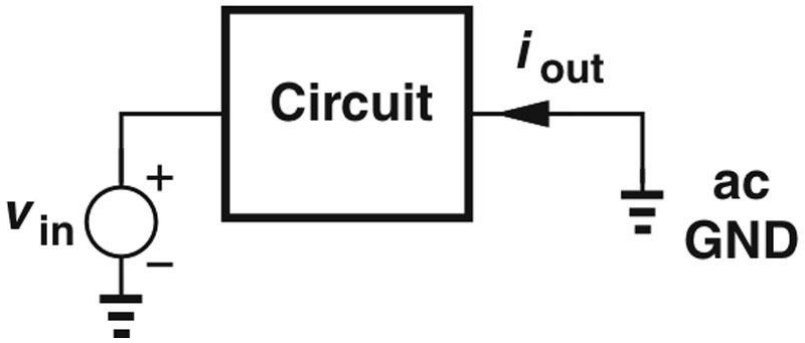
$$R_{out} = (1 + g_{m1} r_{O2}) r_{O1} + r_{O2} \approx g_{m1} r_{O1} r_{O2},$$

intrinsic gain

Stacking M_1 atop M_2 to raise R_{out}



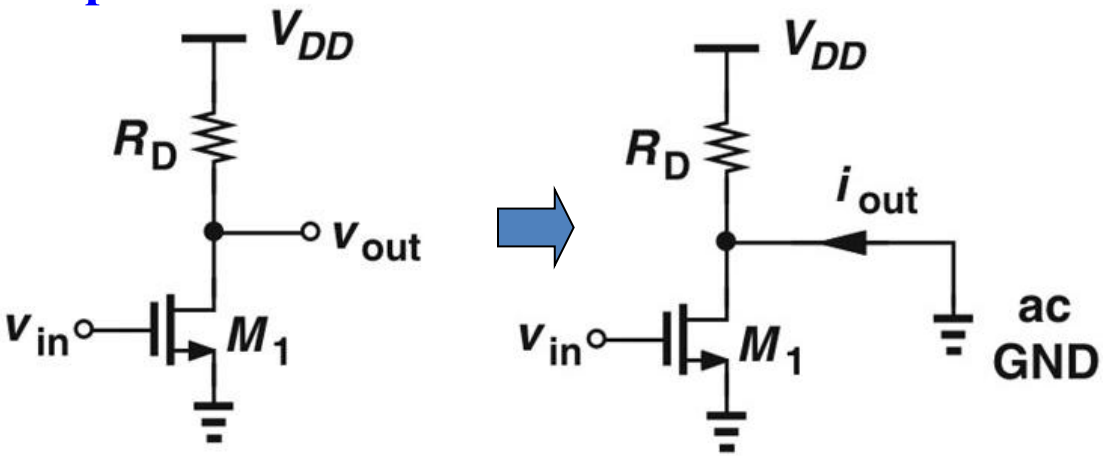
Short-Circuit Transconductance



$$G_m = \left.\frac{i_{out}}{v_{in}}\right|_{v_{out}=0}$$

- **The short-circuit transconductance of a circuit measures its strength in converting input voltage to output current.**

<Example 9.7> Calculate the transconductance of the CS stage.

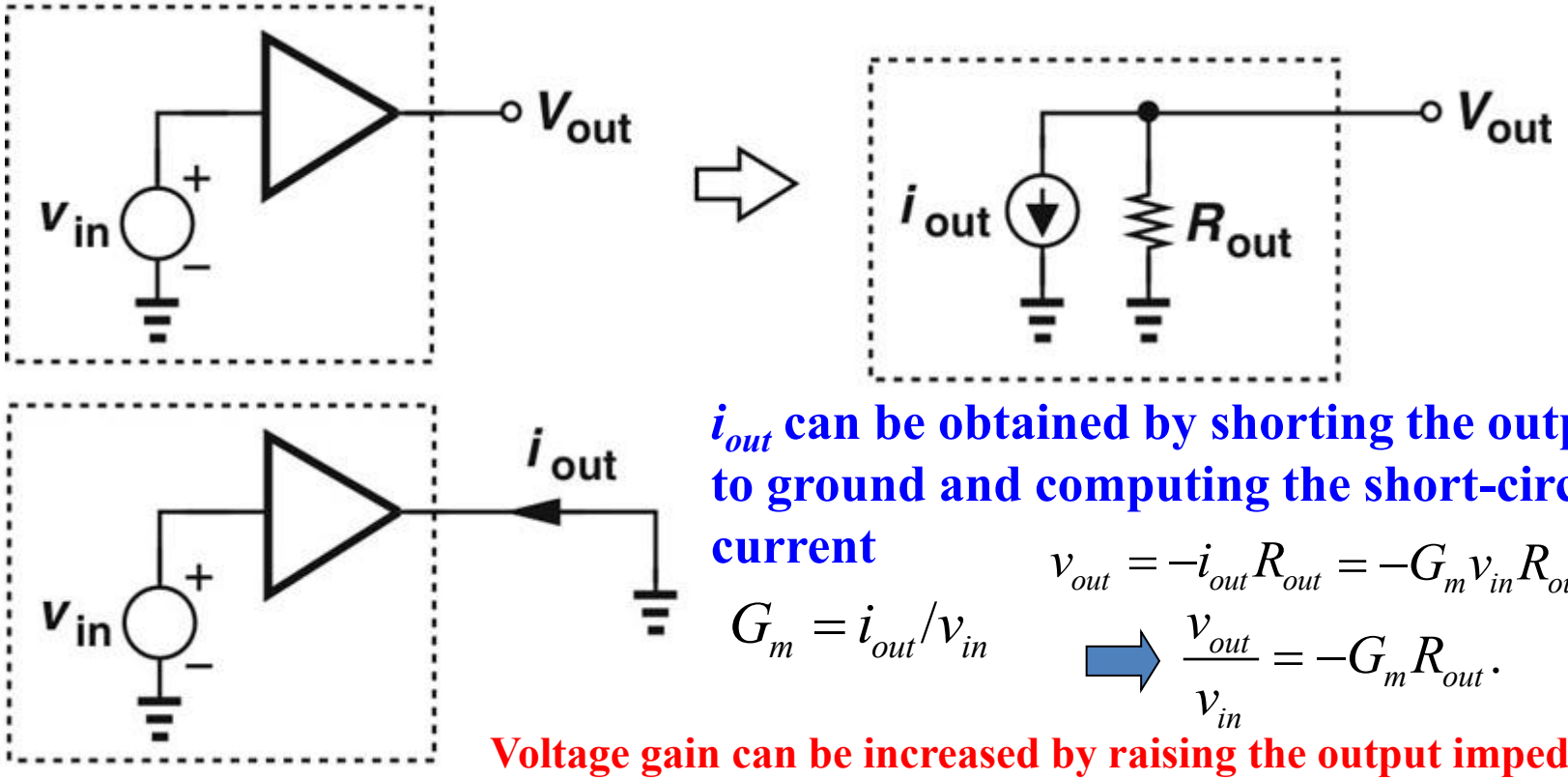


$$G_m = \frac{i_{out}}{v_{in}} = \frac{i_{D1}}{v_{GS1}} = g_{m1}.$$

Voltage Gain of Linear Circuit

<Lemma> The voltage gain of a linear circuit can be expressed as $A_v = -G_m R_{out}$, where R_{out} denotes the output resistance of the circuit.

A linear circuit can be replaced with its Norton equivalent



i_{out} can be obtained by shorting the output to ground and computing the short-circuit current

$$G_m = i_{out}/v_{in}$$

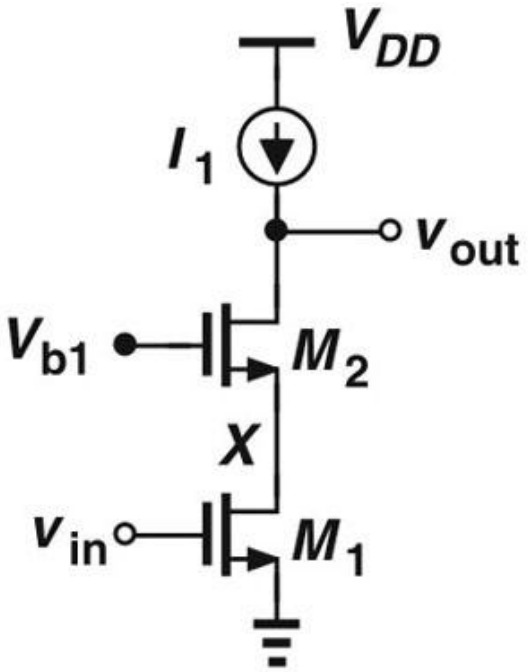
$$v_{out} = -i_{out} R_{out} = -G_m v_{in} R_{out}$$

$$\Rightarrow \frac{v_{out}}{v_{in}} = -G_m R_{out}.$$

Voltage gain can be increased by raising the output impedance!!

MOS Cascode Amplifier

With ideal current source load

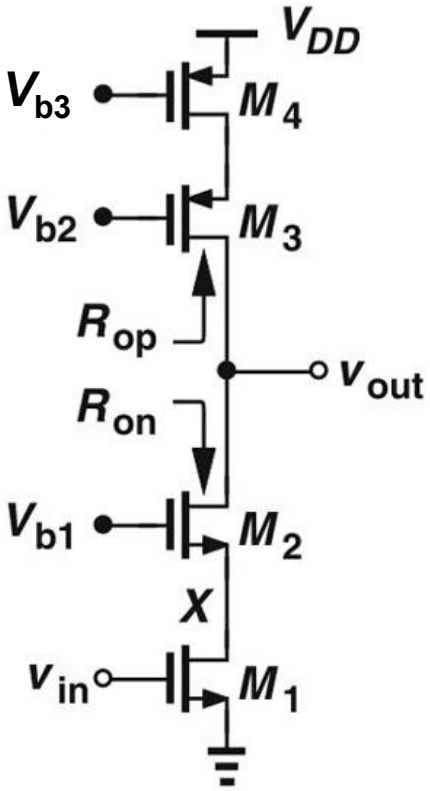


$$A_v = -G_m R_{out}$$

$$\approx -g_{m1}[(1+g_{m2}r_{O2})r_{O1} + r_{O2}]$$

$$\approx -g_{m1}r_{O1}g_{m2}r_{O2}.$$

With a PMOS cascode current source load



$$R_{on} \approx g_{m2}r_{O2}r_{O1}$$

$$R_{op} \approx g_{m3}r_{O3}r_{O4}.$$

$$A_v \approx -g_{m1}[(g_{m2}r_{O2}r_{O1}) \| (g_{m3}r_{O3}r_{O4})].$$

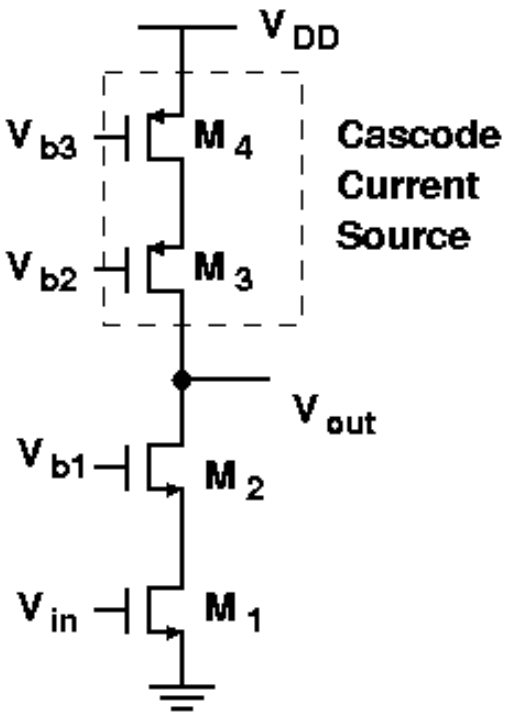
NMOS CAS Amp + PMOS CAS Load

- Cascode as a constant current source with high output impedance
- The maximum output swing is equal to

$$V_{out,swing} = V_{DD} - V_{DS1} - V_{DS2} - V_{SD3} - V_{SD4}$$

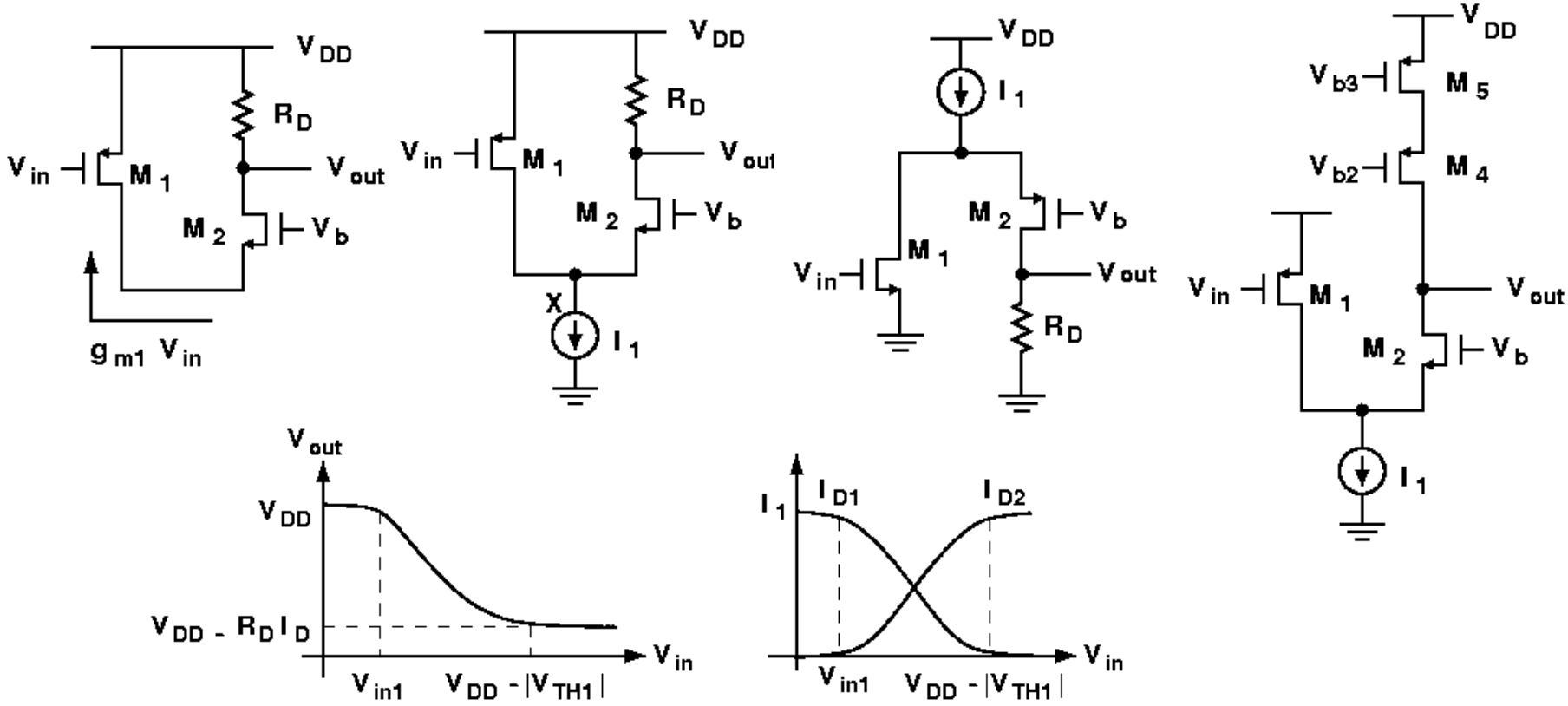
$$R_{out} = \{\left[1 + \left(g_{m2} + g_{mb2}\right) r_{O2}\right] r_{O1} + r_{O2}\} \\ \| \{\left[1 + (g_{m3} + g_{mb3}) r_{O3}\right] r_{O4} + r_{O3}\}$$

$$A_v \approx -g_{m1}\left[\left(g_{m2} r_{O2} r_{O1}\right) \| \left(g_{m3} r_{O3} r_{O4}\right)\right]$$

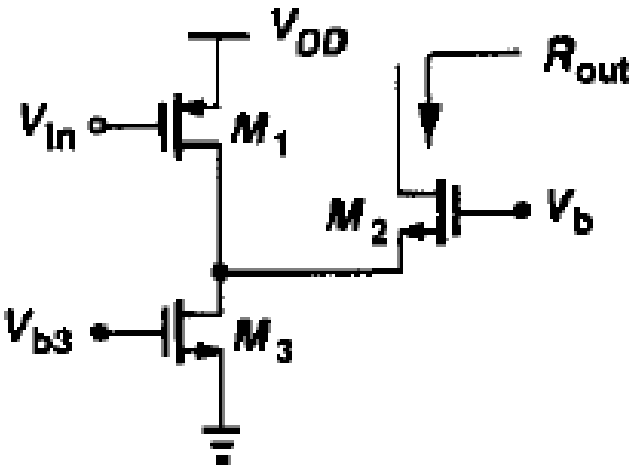


Folded Cascode

- A PMOS-NMOS combination.
- The total bias current in this case must be higher to achieve comparable performance.



R_{out} of Folded-Cascode



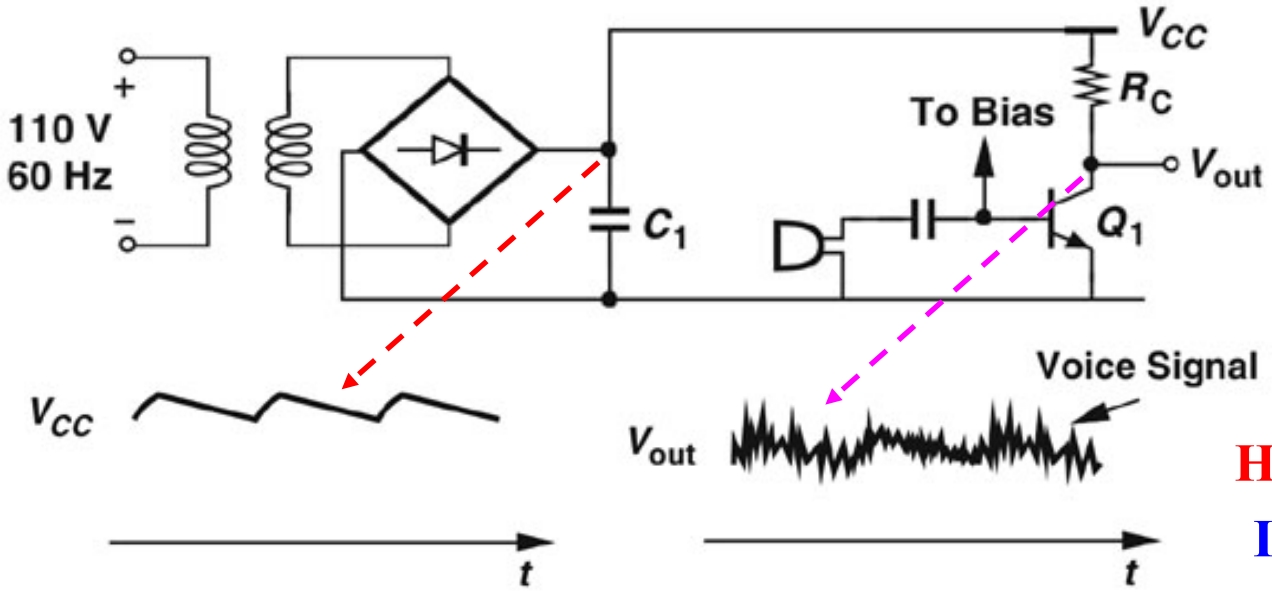
$$R_{out} = \left[1 + \left(g_{m2} + g_{mb2}\right) r_{O2}\right] \left(r_{O1} \| r_{O3}\right) + r_{O2}$$

Elementary Gain Stages

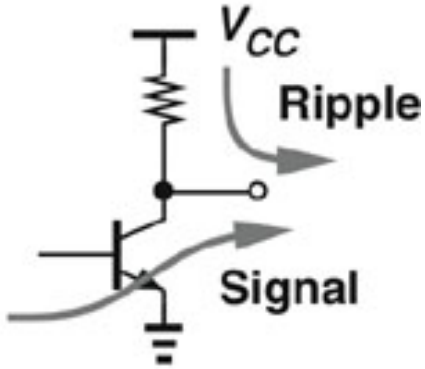
- Current Source and Biasing
- CMOS Amplifiers (CS, CG, CD, Cascode)
- Differential Amplifiers

Example 10.1: Audio Amplifier

A student constructs a circuit to amplify the signal produced by a microphone. Upon applying the result to a speaker, he observes that the amplifier output contains a strong "humming" noise, a steady low-frequency component. Why?



Two paths to output



How do we suppress hum?

Increase C_1? Too large!!

The current drawn from the rectified output creates a ripple waveform at twice the ac line frequency (Ch3)

(1) The amplified version of the microphone signal

(2) The ripple waveform present on V_{CC}

$$V_{out} = V_{CC} - R_C I_C,$$

V_{out} tracks V_{CC}!!

Remove Effect of Ripple

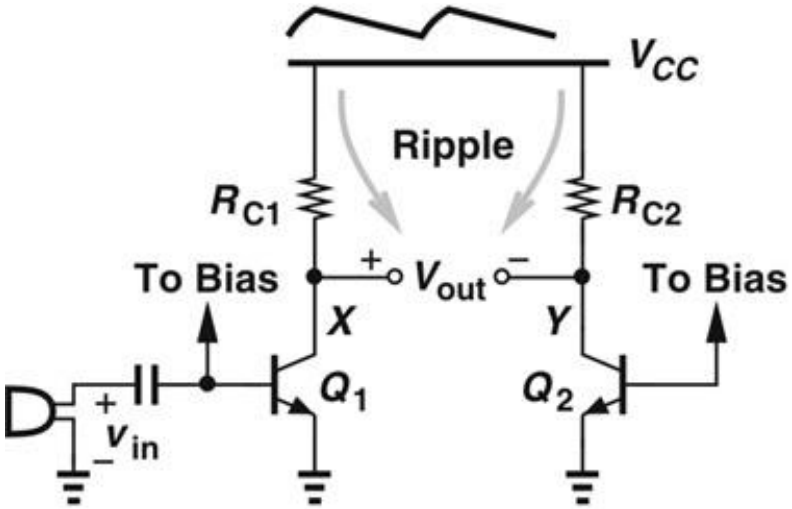
Modify the amplifier topology such that the output is insensitive to V_{CC}. How ??

$V_{out} = V_{CC} - R_C I_C$, Both V_{out} and V_{CC} are measured respect to ground

What if V_{out} is not "referenced" to ground?!

What if V_{out} is "referenced" to another point that experiences the supply ripple?

Implement the concept

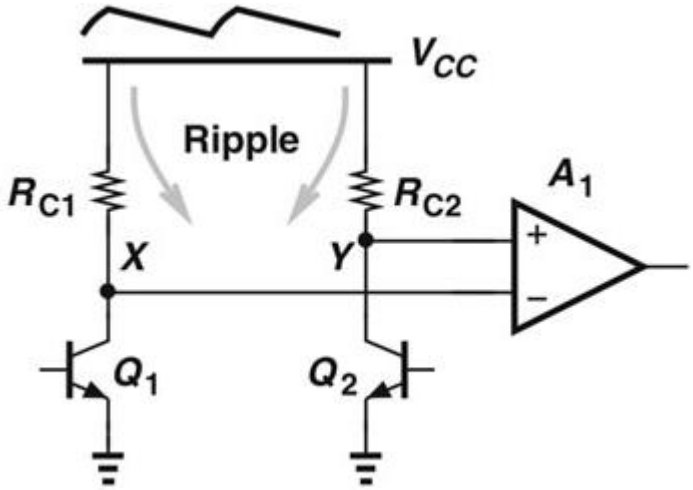


$$v_X = A_v v_{in} + v_r$$

$$v_Y = v_r.$$

$$v_X - v_Y = A_v v_{in}.$$

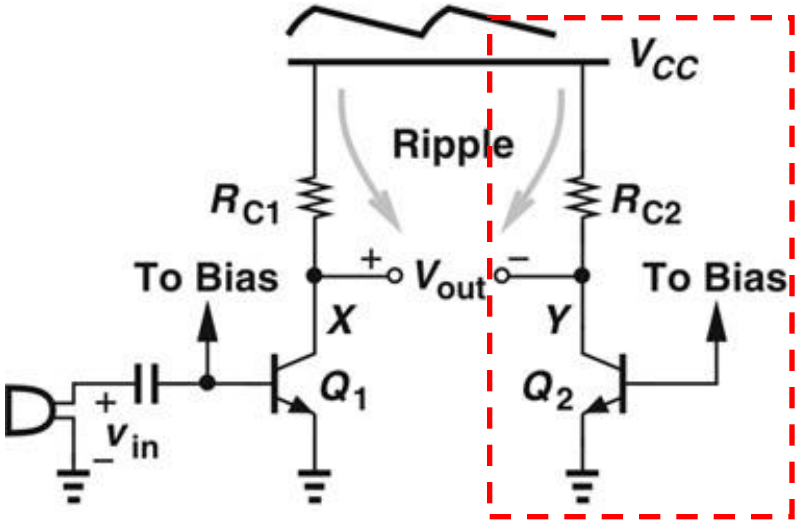
Ripple-free differential output



The *difference* between V_X and V_Y remains free from the ripple!!

The symmetric CE stages provide two output nodes whose voltage difference remains free from the supply ripple

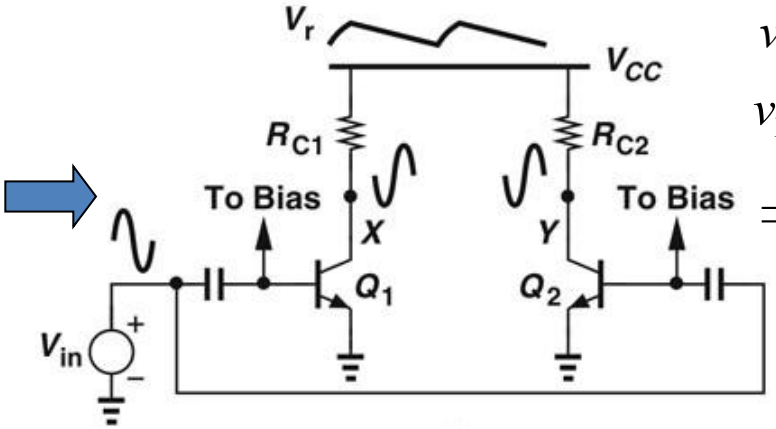
Waste vs. Benefit



Wasting current!!

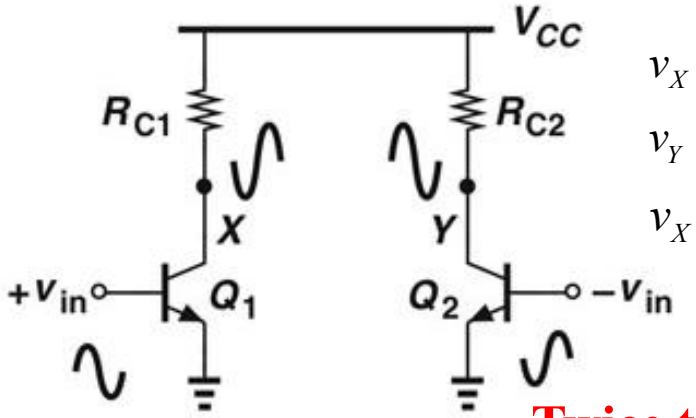
Can it provide some amplification?

Apply signal to Q_{2B}



$$v_X = A_v v_{in} + v_r$$
$$v_Y = A_v v_{in} + v_r$$
$$\Rightarrow v_X - v_Y = 0.$$

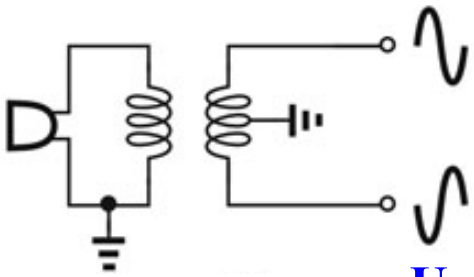
Invert one input



$$v_X = A_v v_{in} + v_r$$
$$v_Y = -A_v v_{in} + v_r$$
$$v_X - v_Y = 2A_v v_{in}.$$

Twice the output!

Generation of differential phases



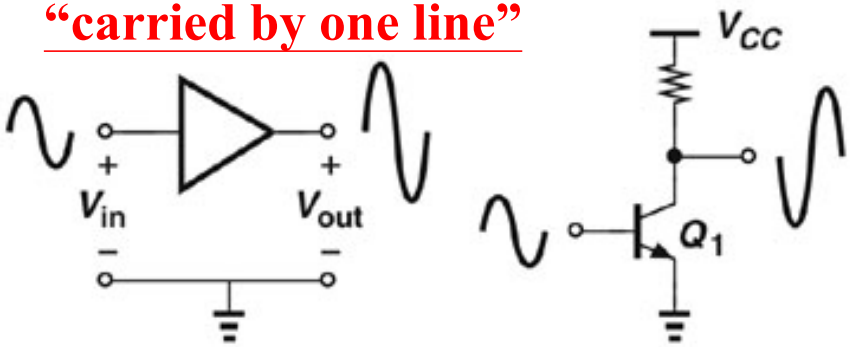
Use a transformer

Single-ended vs. Differential

Single-ended signals:

measured with respect to the common ground

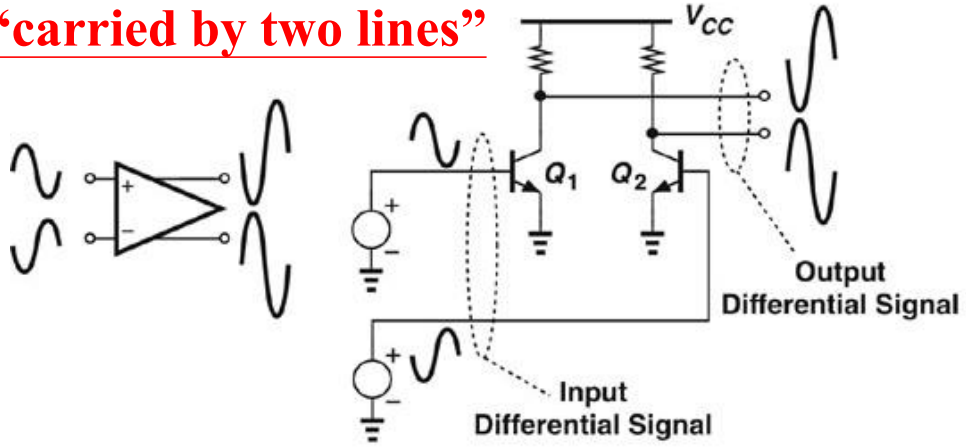
"carried by one line"



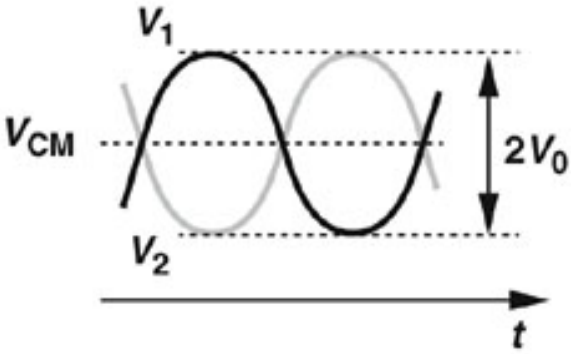
Differential signals:

measured between two nodes that have equal and opposite swings

"carried by two lines"



Illustration

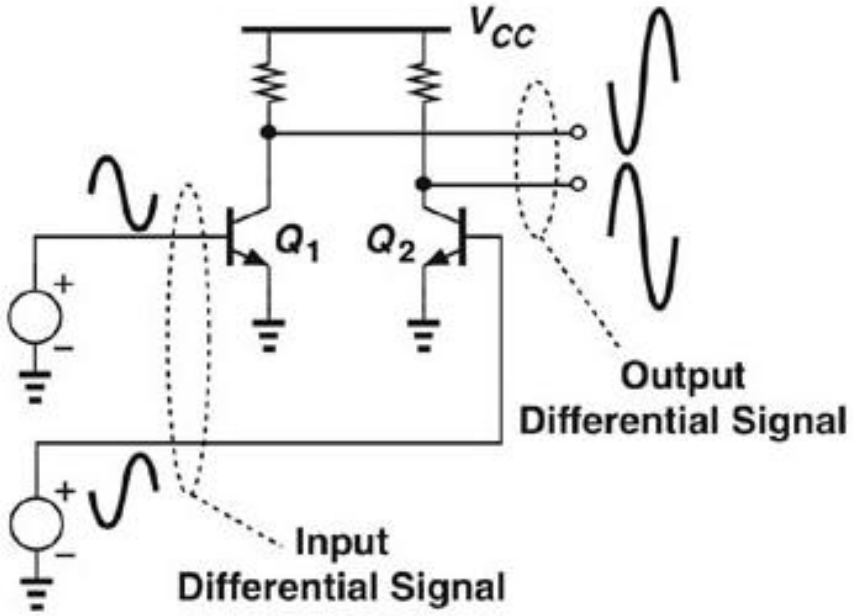


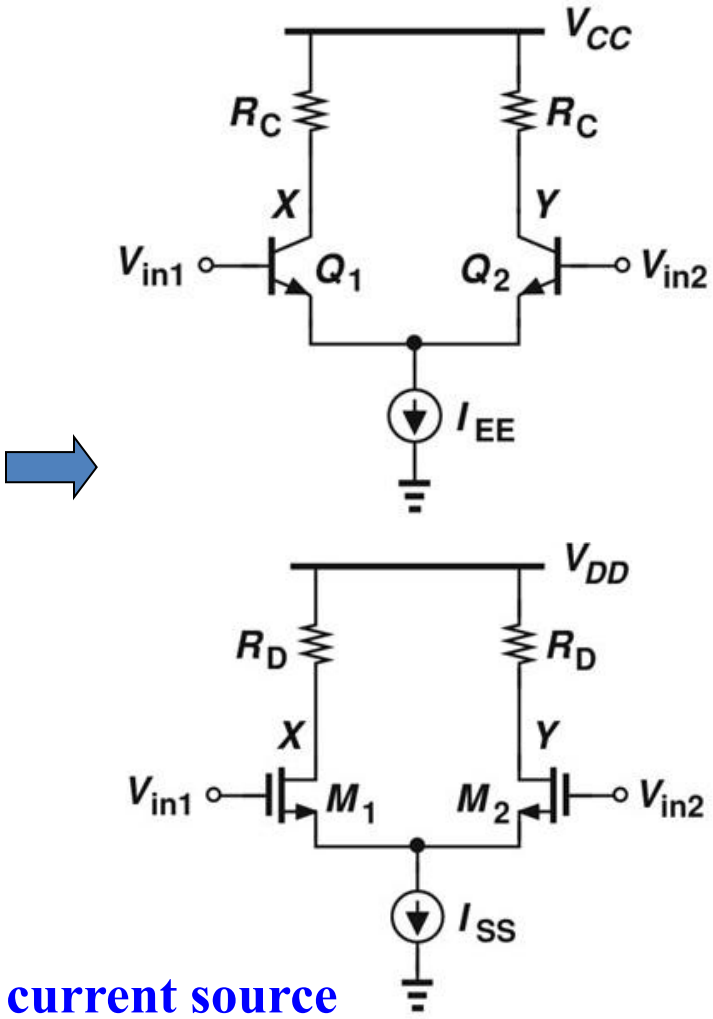
$$V_1 = V_0 \sin \omega t + V_{CM}$$
$$V_2 = -V_0 \sin \omega t + V_{CM}$$

V_1 and V_2: differential signals

V_{CM}: the "common-mode (CM) level"

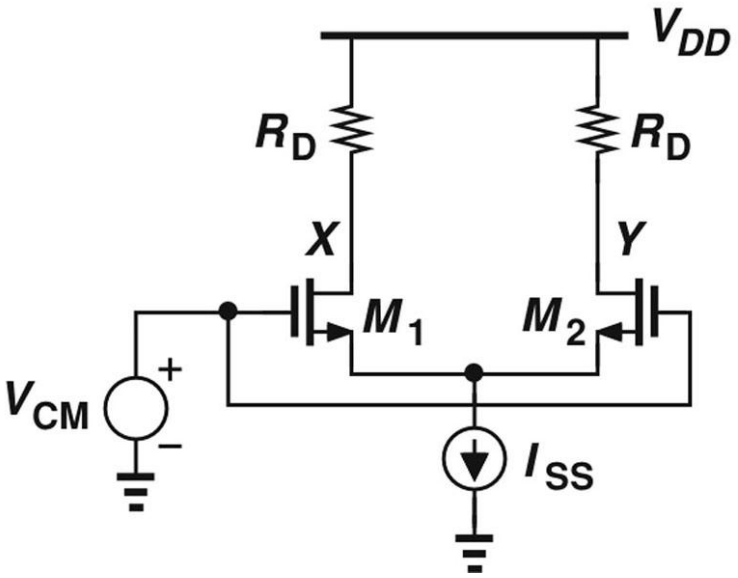
Differential Pair





I_{EE} and I_{SS}: tail current source

MOSFET Differential Pair



Equilibrium overdrive voltage:

$$\lambda = 0 \qquad I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})^2$$

$$\Rightarrow \quad (V_{GS} - V_{TH})_{equil.} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox}\dfrac{W}{L}}}.$$

$$I_{D1} = I_{D2} = \frac{I_{SS}}{2}$$

$$V_X = V_Y = V_{DD} - R_D\frac{I_{SS}}{2}.$$

For M_1 and M_2 to operate in saturation:

$$V_{DD} - R_D\frac{I_{SS}}{2} > V_{CM} - V_{TH}.$$

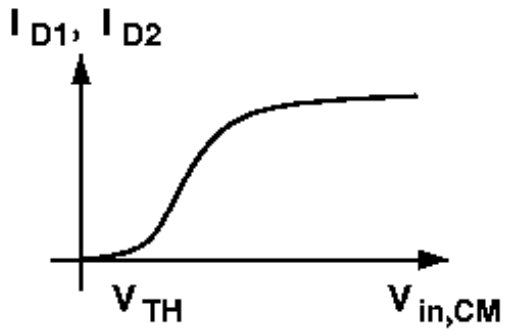
V_{CM} could be higher than V_{DD} !!

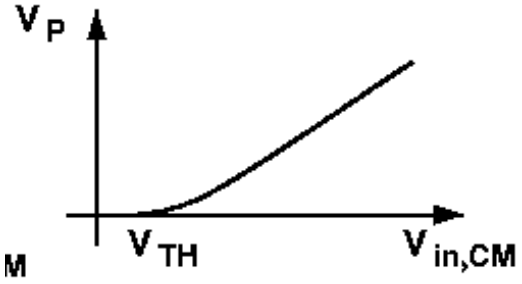
- **Similar to its bipolar counterpart, MOS differential pair produces zero differential output as V_{CM} changes.**

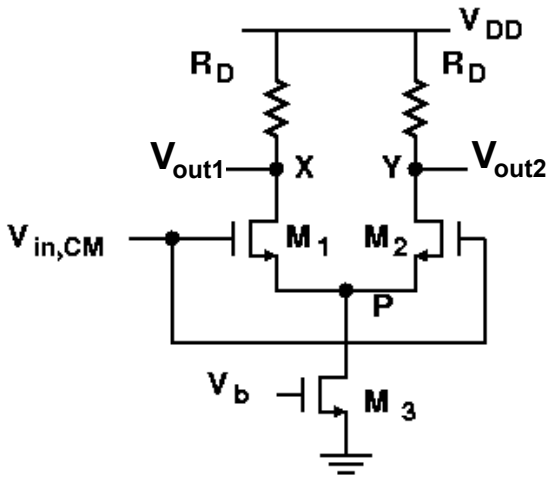
Input Common-Mode Range

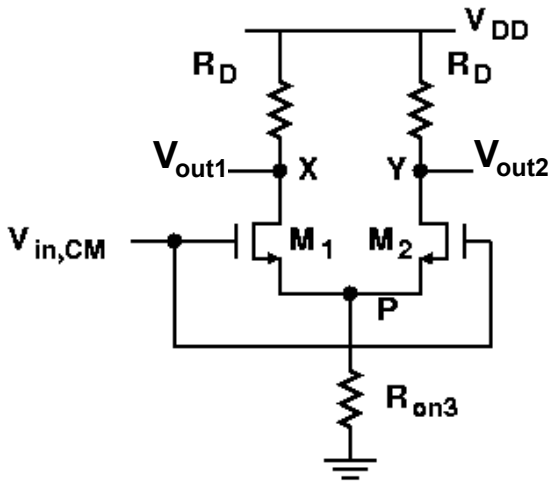
- The tail current source is to suppress the effect of input CM level variations.
- For proper operation, M1, M2 and M3 should be operated in saturation region.
- If $V_{in,CM}$ rises further, then M1 and M2 will enter the triode region.

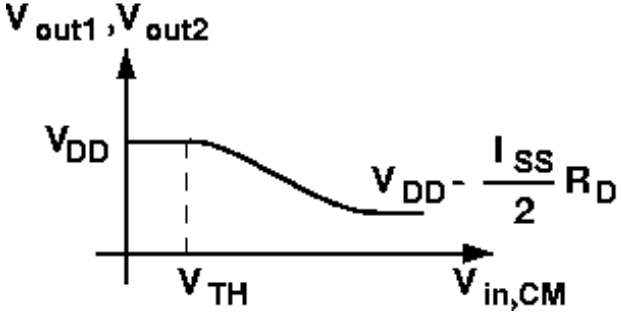
$$V_{GS1} + (V_{GS3} - V_{TH3}) \le V_{in,CM} \le \min\left[V_{DD} - R_D \frac{I_{SS}}{2} + V_{TH}, V_{DD} \right]$$



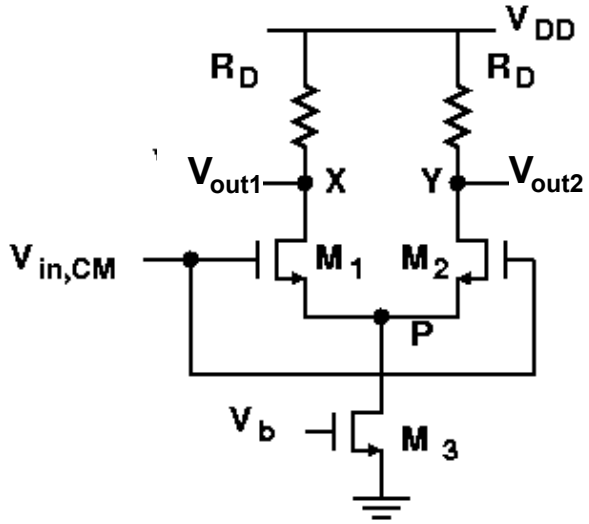


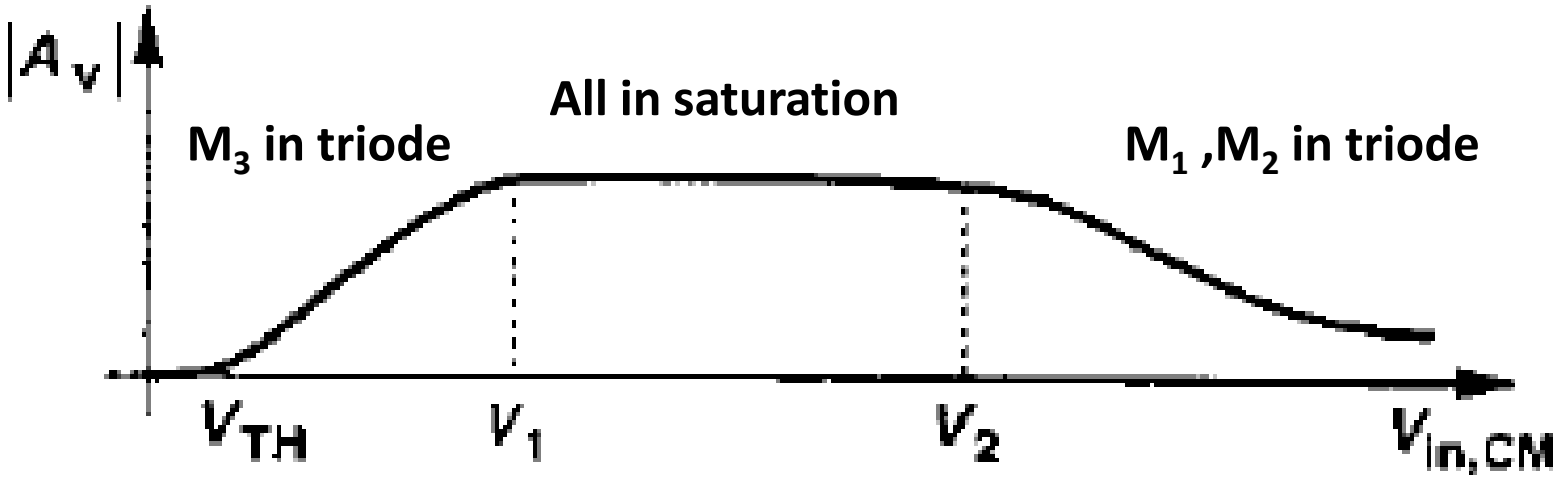




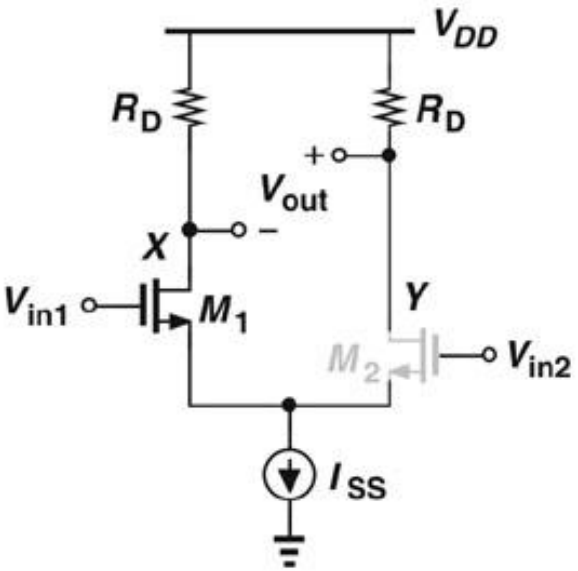


A_v vs. $V_{in.CM}$

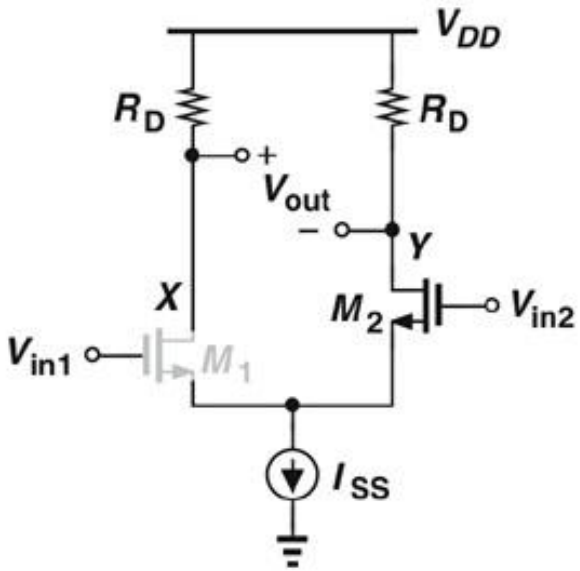

V DD
R D
R D
V out1
X
Y
V out2
V in,CM
M 1
M 2
P
V b
M 3


|A v|
All in saturation
M3 in triode
M1 ,M2 in triode
V TH
V 1
V 2
V in,CM

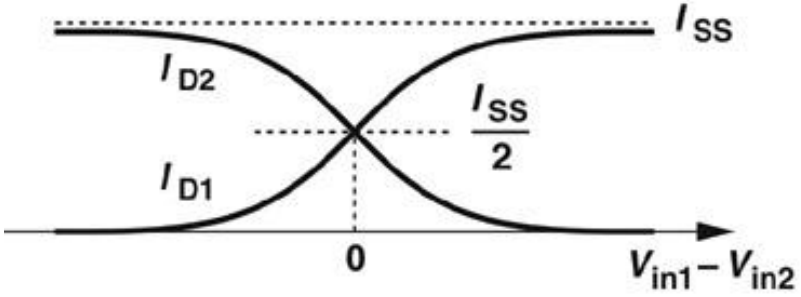
Large-Signal Response

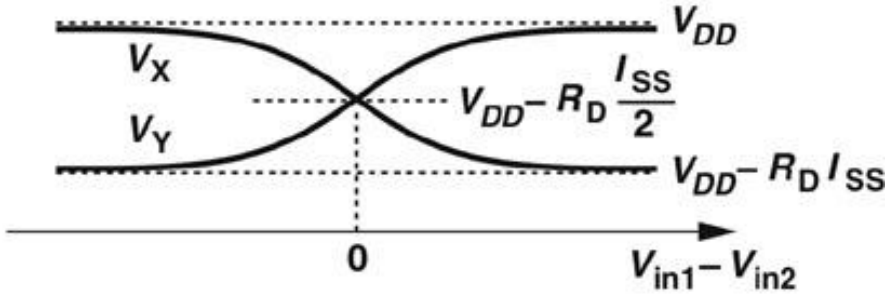


(a)



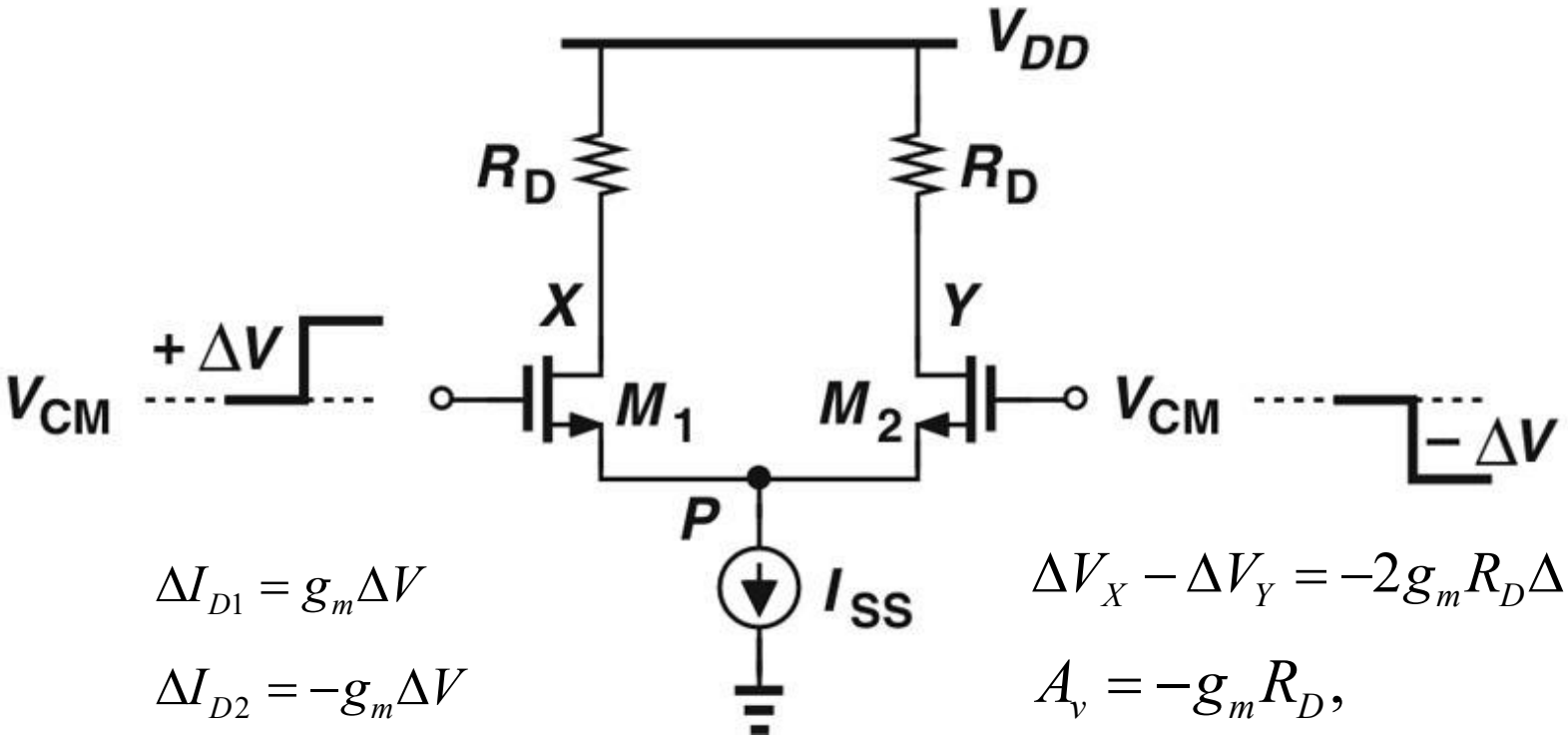
(b)





(c)

Small-Signal Response



$$\Delta I_{D1} = g_m \Delta V$$

$$\Delta I_{D2} = -g_m \Delta V$$

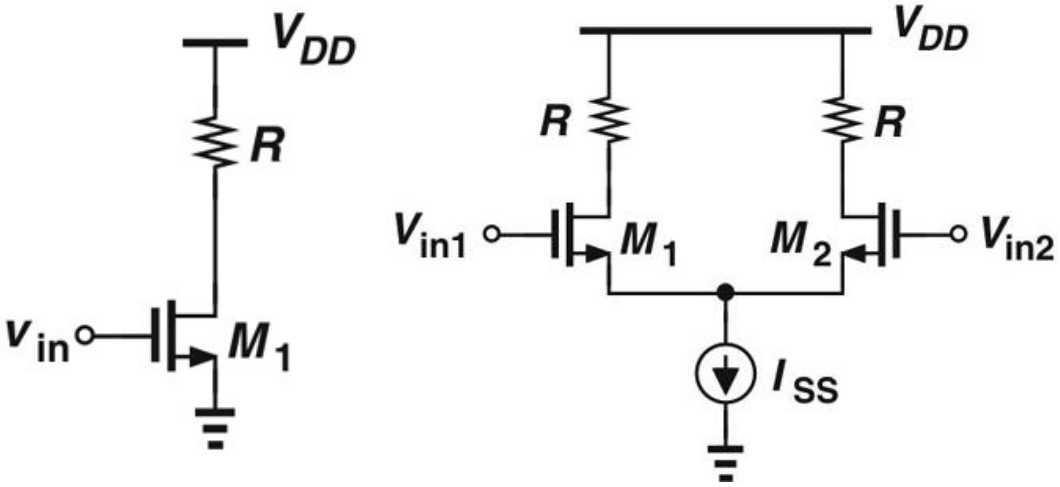
$$\Delta V_X - \Delta V_Y = -2 g_m R_D \Delta V.$$

$$A_v = -g_m R_D,$$

- **Similar to its bipolar counterpart, the MOS differential pair exhibits the same virtual ground node and small signal gain.**

Example 10.18

The common source amplifier and the differential pair incorporate equal load resistors. If the two circuits are designed for the same voltage gain and the same supply voltage, discuss the choice of (a) transistor dimensions for a given power budget, (b) power dissipation for given transistor dimensions



(a) For a given power budget

$$I_{D1} = I_{SS} = 2I_{D2} = 2I_{D3}$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}.$$

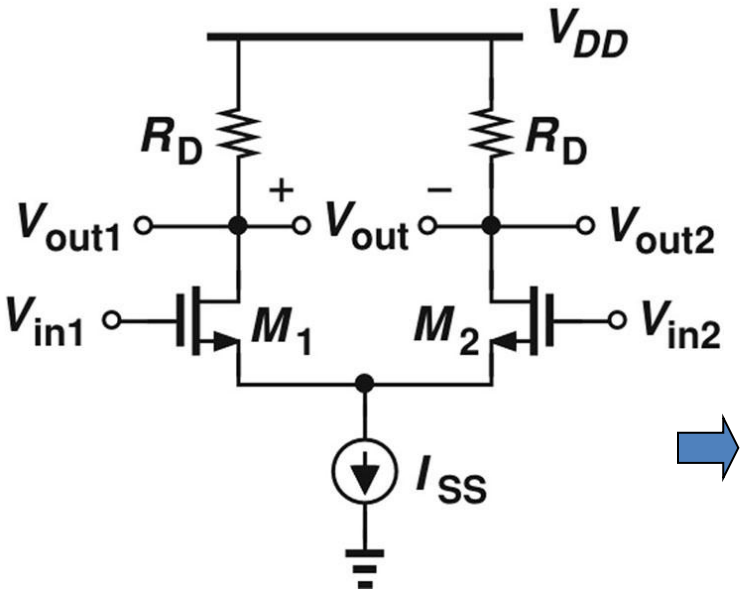
$$\Rightarrow \quad \left(\frac{W}{L}\right)_{diff} = 2\left(\frac{W}{L}\right)_{CS}$$

(b) For a given dimension

$$I_{SS} = 2I_{CS}$$

$$P_{diff} = 2P_{CS}$$

Large-Signal Analysis



$$I_{D1} = \frac{I_{SS}}{2} + \frac{V_{in1} - V_{in2}}{4}\sqrt{\mu_n C_{ox}\frac{W}{L}\left[4I_{SS} - \mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})^2\right]}.$$

$$I_{D2} = \frac{I_{SS}}{2} + \frac{V_{in2} - V_{in1}}{4}\sqrt{\mu_n C_{ox}\frac{W}{L}\left[4I_{SS} - \mu_n C_{ox}\frac{W}{L}(V_{in2} - V_{in1})^2\right]}.$$

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}.$$

$$V_{out} = V_{out1} - V_{out2} = -R_D(I_{D1} - I_{D2}).$$

$$V_{in1} - V_{GS1} = V_{in2} - V_{GS2}$$

$$I_{D1} + I_{D2} = I_{SS}.$$

$$I_D = (1/2)\mu_n C_{ox}(W/L)(V_{GS} - V_{TH})^2$$

$$\Rightarrow \quad V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}}.$$

For I_{D1}- I_{D2} = 0

(a) V_{in1}-$V_{in2} = 0$

(b) $(V_{in1} - V_{in2})^2 = 4I_{SS}/(\mu_n C_{ox} W/L)$

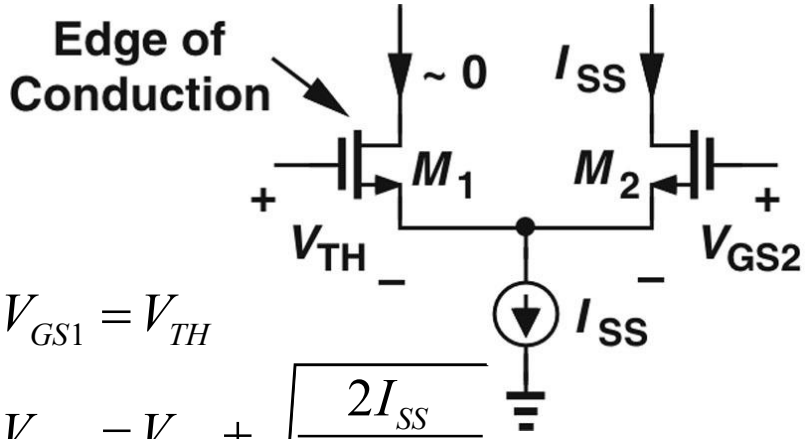
(c) $(V_{in1} - V_{in2})^2 > 4I_{SS}/(\mu_n C_{ox} W/L)$?????

How should these results be interpreted?

One Device is OFF

We assumed that both transistors are *on*

Determine the input difference that places one transistor at the edge of conduction

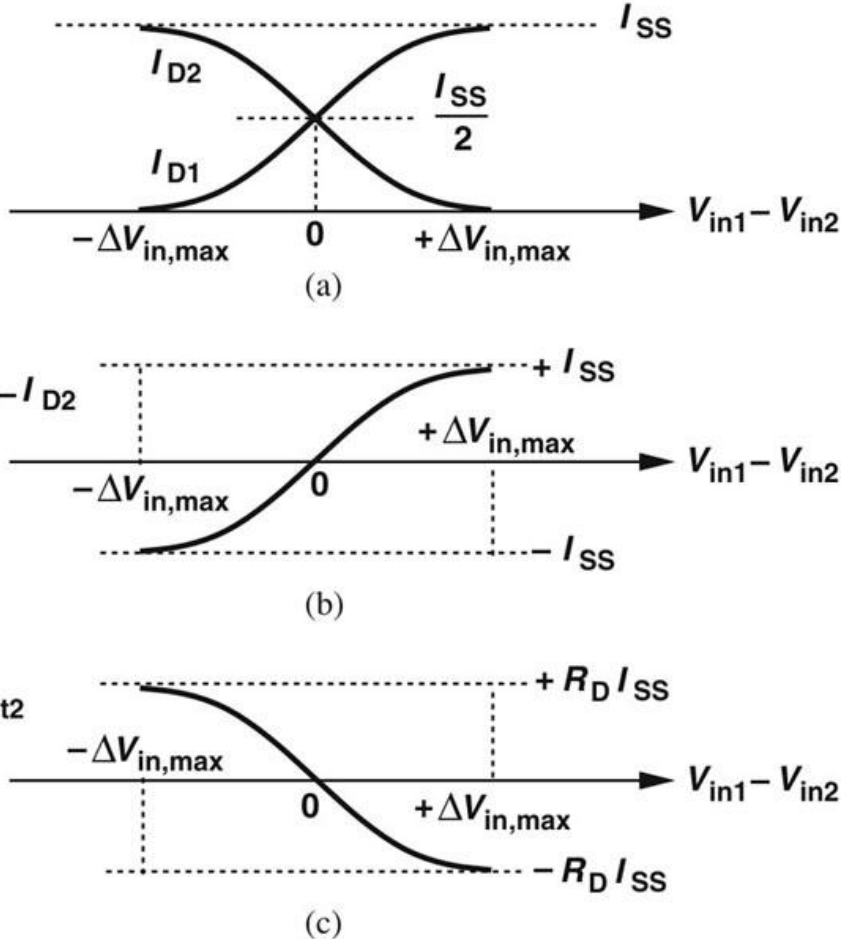


$$V_{GS1} = V_{TH}$$

$$V_{GS2} = V_{TH} + \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}.$$

$$\Rightarrow \; |V_{in1} - V_{in2}|_{max} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}},$$

$$|V_{in1} - V_{in2}|_{max} = \sqrt{2}(V_{GS} - V_{TH})_{equil.}.$$



Small-Signal Analysis

$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}} - (V_{in1} - V_{in2})^2}.$$

Define small signal as: $|V_{in1} - V_{in2}| << \dfrac{4I_{SS}}{\mu_n C_{ox}\dfrac{W}{L}}$

Differential inputs and outputs are *linearly* proportional

$$\Rightarrow \quad I_{D1} - I_{D2} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} = \sqrt{\mu_n C_{ox}\frac{W}{L}I_{SS}}\,(V_{in1} - V_{in2}).$$

Small-signal equivalent circuit

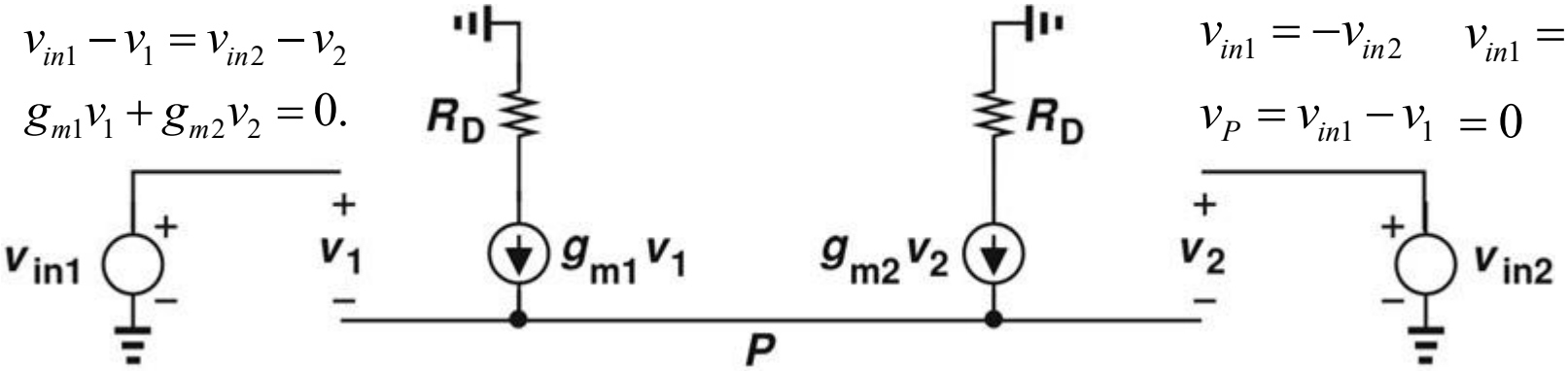
$$v_{in1} - v_1 = v_{in2} - v_2$$

$$g_{m1}v_1 + g_{m2}v_2 = 0.$$

$$v_1 = -v_2$$

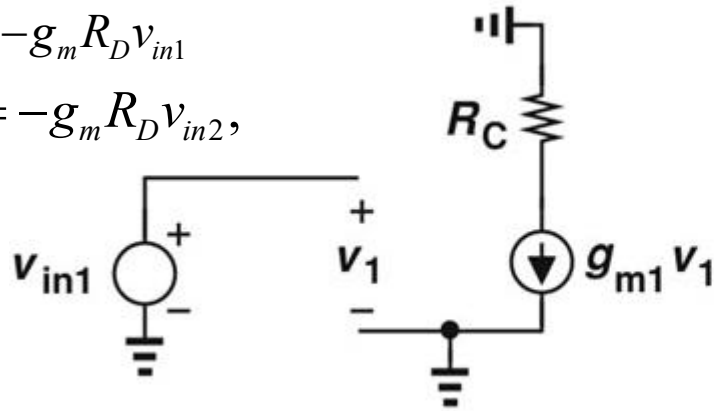
$$v_{in1} = -v_{in2} \qquad v_{in1} = v_1$$

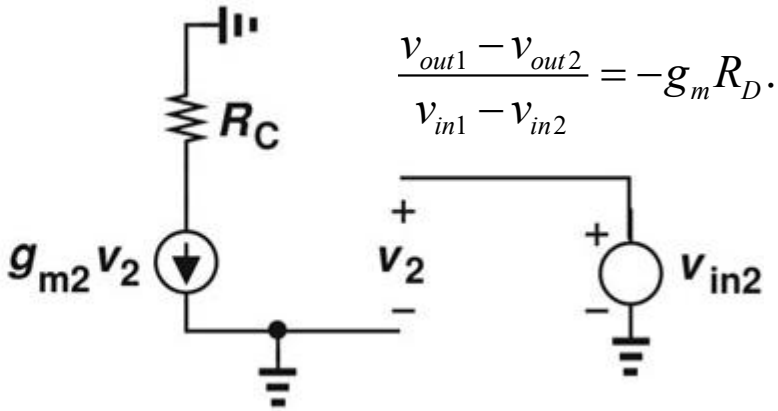
$$v_P = v_{in1} - v_1 = 0$$



Virtual Ground and Half Circuit

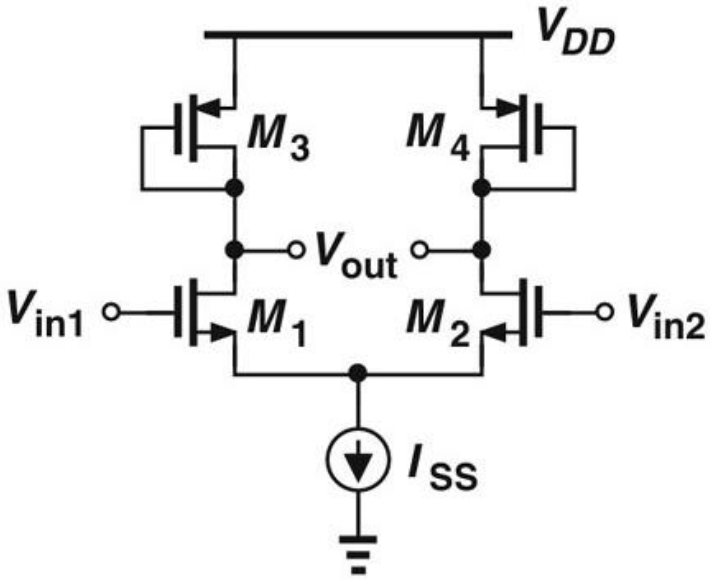
$$v_{out1} = -g_m R_D v_{in1}$$
$$v_{out2} = -g_m R_D v_{in2},$$

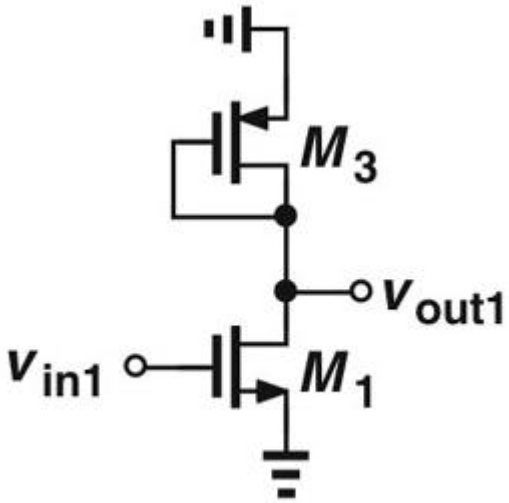




$$\frac{v_{out1} - v_{out2}}{v_{in1} - v_{in2}} = -g_m R_D.$$

<Example 10.22> Determine the voltage gain of the circuit. Assume λ≠0.

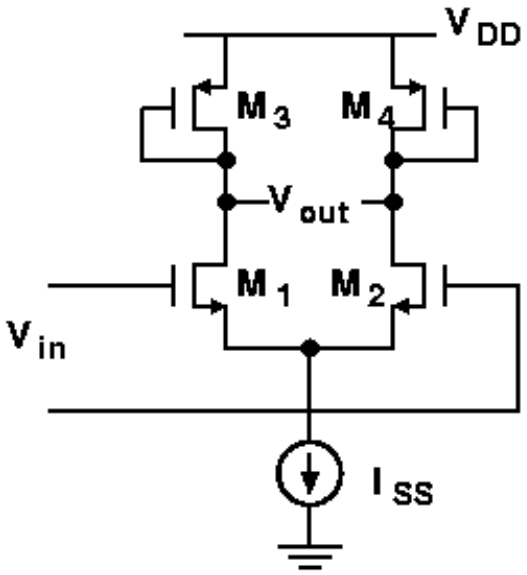




$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \| r_{O3} \| r_{O1}\right).$$

Differential Pair with MOS Loads

- Diode load

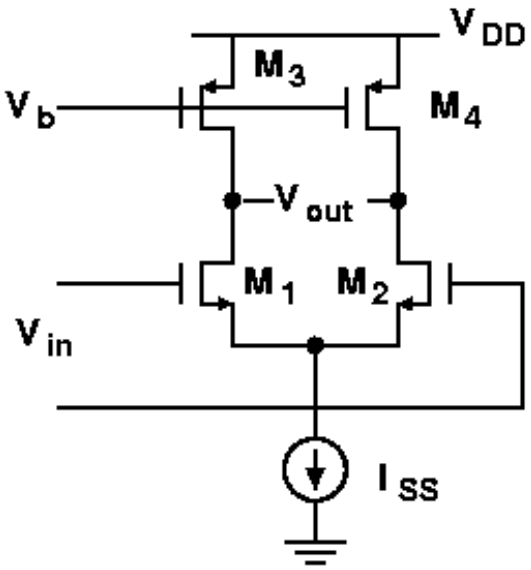


$$A_v = -g_{mN}\left(g_{mP}^{-1} \,||\, r_{ON} \,||\, r_{OP}\right)$$

$$\approx -\frac{g_{mN}}{g_{mP}} \approx -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$

Output CM level = V_{DD} - V_{GSP}

- Current source load

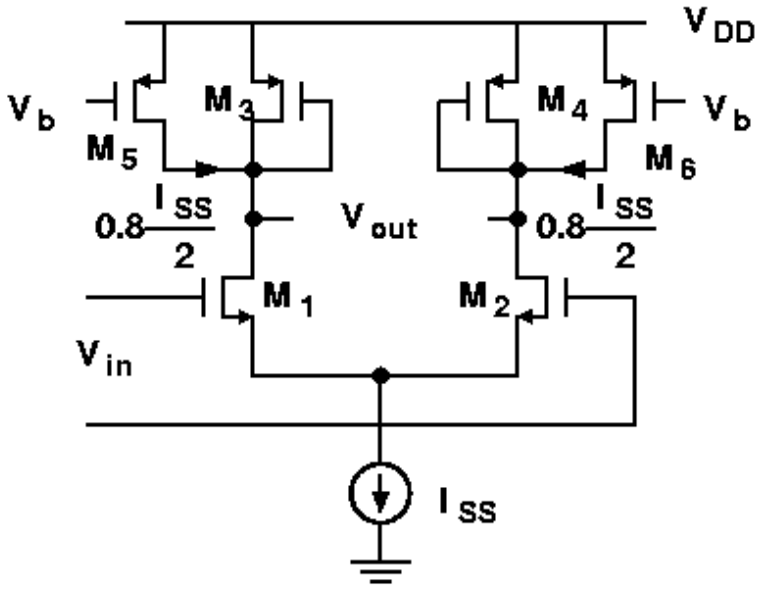


$$A_v = -g_{mN}\left(r_{ON} \,||\, r_{OP}\right)$$

Output CM not well defined
Need CM Feedback circuit

Differential Pair with MOS Loads

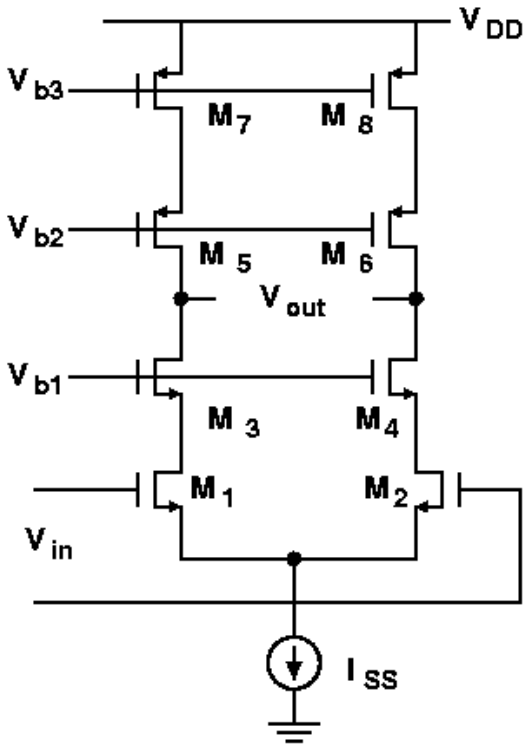
- Addition of current sources to increase the voltage gain



$$I_D(\mathrm{M}_3, \mathrm{M}_4) = 0.2\frac{I_{SS}}{2} \ ,$$

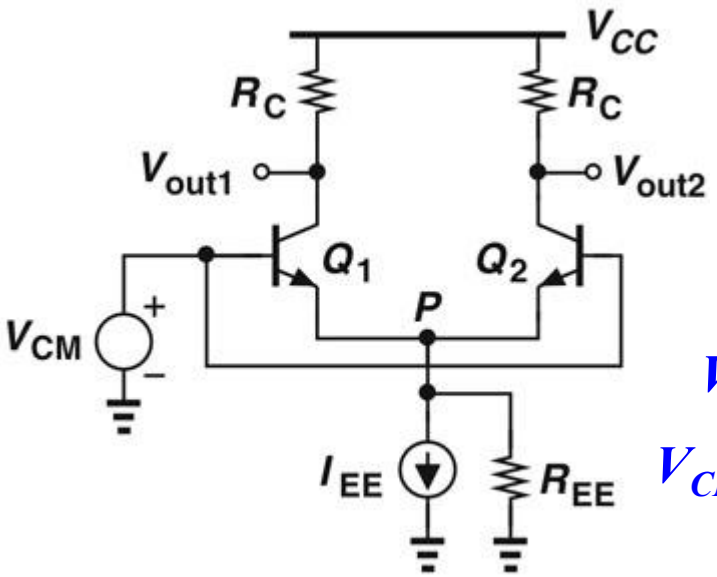
$g_m(\mathrm{M}_3, \mathrm{M}_4)$ decresed to be 1/5, Gain increased x5

- Cascode differential pair

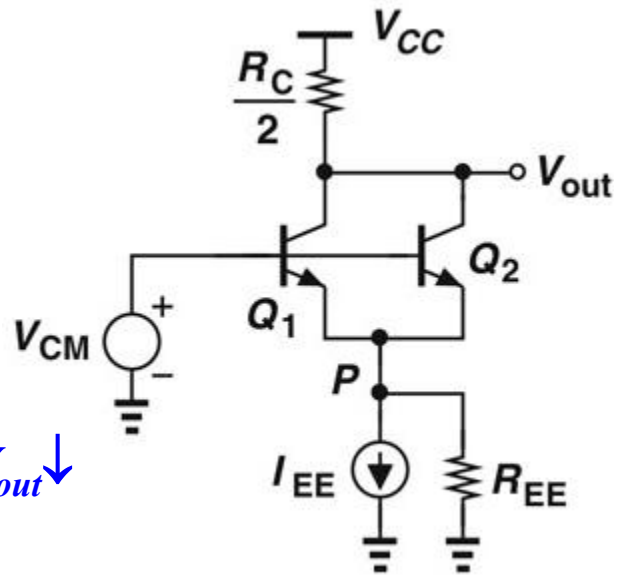


$$A_v \approx -g_{m1}\left[(g_{m3}r_{O3}r_{O1}) \,||\, (g_{m5}r_{O5}r_{O7})\right]$$

Finite Tail Impedance



$$V_{out1} = V_{out2}$$



V_P follows V_{CM}

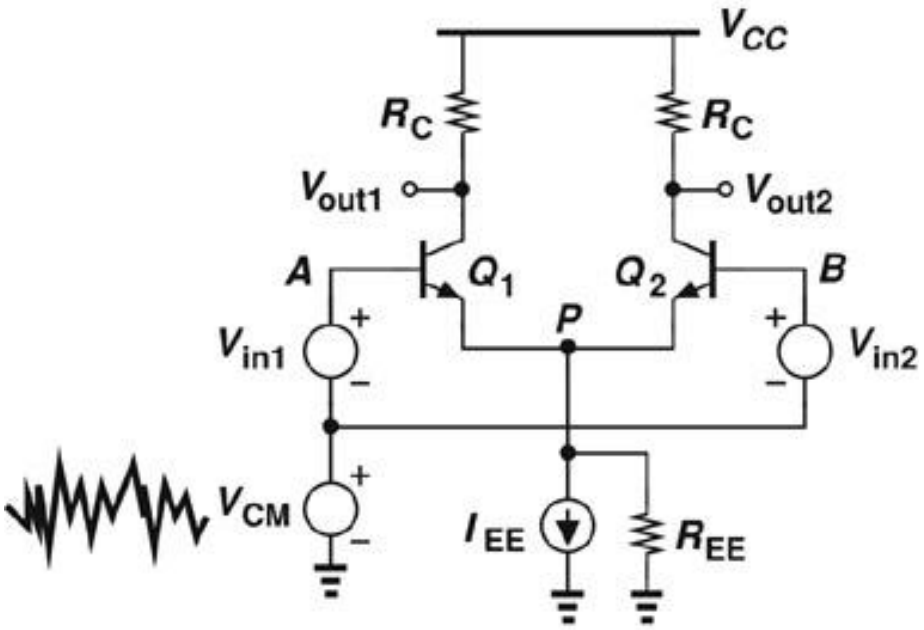
$V_{CM}\uparrow$, $V_P\uparrow$, $I\uparrow$, $V_{out}\downarrow$

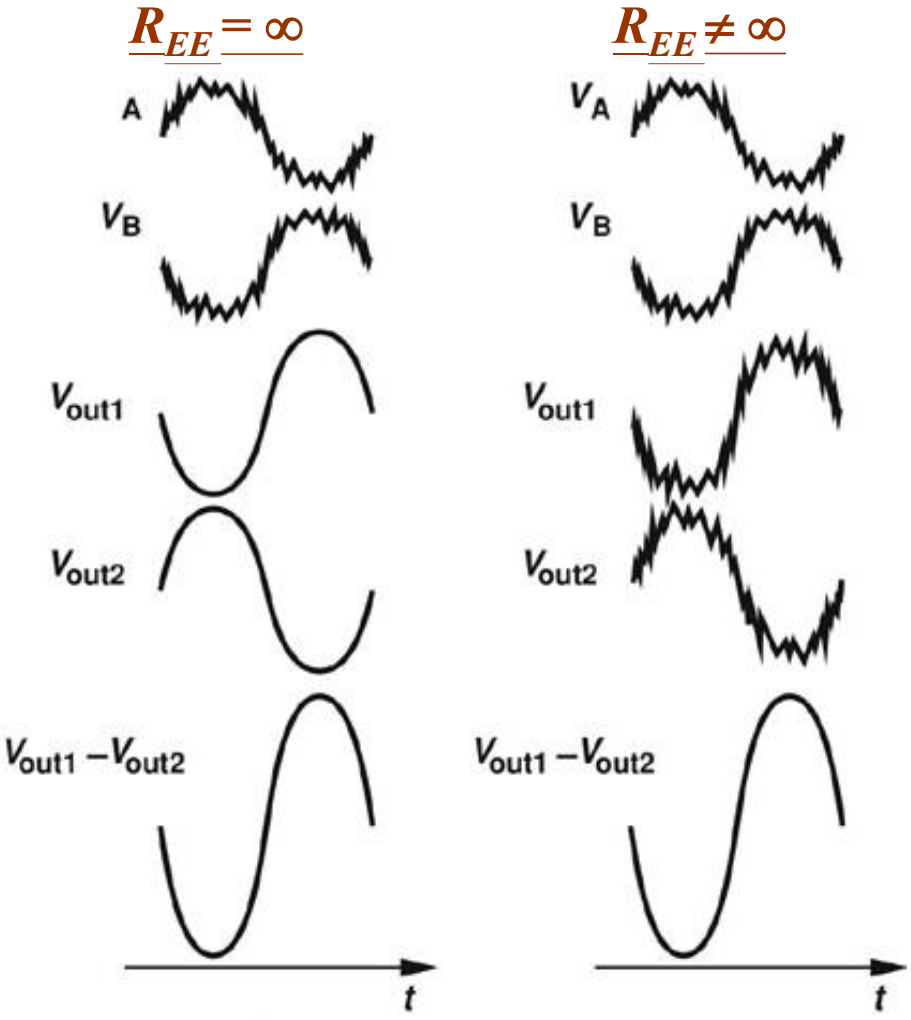
$$\text{Common mode gain} = \frac{\Delta V_{out,CM}}{\Delta V_{in,CM}} = -\frac{\frac{R_C}{2}}{R_{EE} + \frac{1}{2g_m}} = -\frac{R_C}{2R_{EE} + g_m^{-1}},$$

Is it serious??

- **If the tail current source is not ideal, then when a input CM voltage is applied, the currents in Q_1 and Q_2 and hence output CM voltage will change.**

Differential Pair w/ Input CM Noise

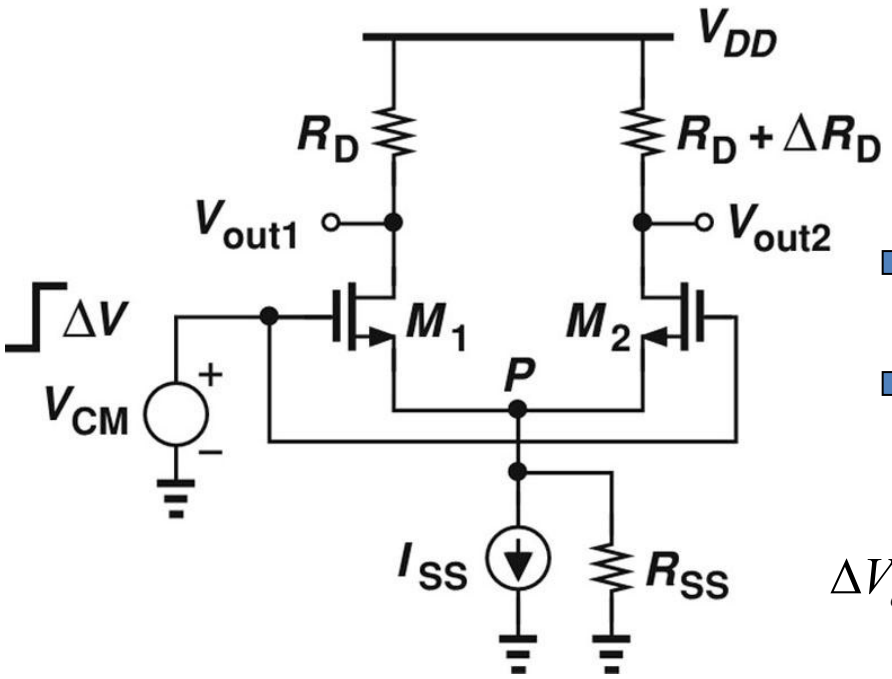




Will cause problem with asymmetries

- **As it can be seen, the differential output voltages for both cases are the same. So for small input CM noise, the differential pair is not affected.**

MOS Pair with Asymmetric Loads



$$\Delta I_{D1} = \Delta I_{D2} = \Delta I_D \qquad \Delta V_{GS1} = \Delta V_{GS2} = \Delta V_{GS}$$

$$\Delta V_{CM} = \Delta V_{GS} + 2\Delta I_D R_{SS} \qquad \Delta V_{GS} = \Delta I_D / g_m$$

$$\Rightarrow \Delta V_{CM} = \Delta I_D \left(\frac{1}{g_m} + 2R_{SS} \right).$$

$$\Rightarrow \Delta I_D = \frac{\Delta V_{CM}}{\frac{1}{g_m} + 2R_{SS}}.$$

$$\Delta V_{out} = \Delta V_{out1} - \Delta V_{out2} = \Delta I_D R_D - \Delta I_D (R_D + \Delta R_D)$$

$$= -\Delta I_D \cdot \Delta R_D = -\frac{\Delta V_{CM}}{\frac{1}{g_m} + 2R_{SS}} \Delta R_D.$$

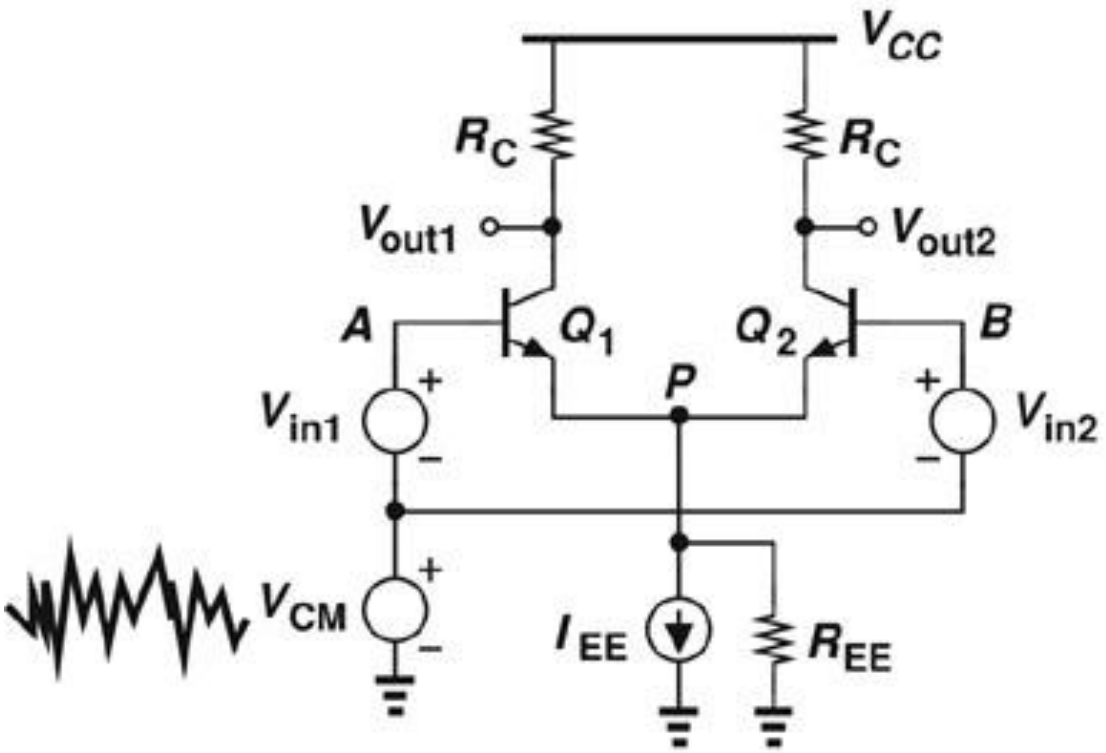
$$I_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{TH})^2$$

$$I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS2} - V_{TH})^2,$$

$$\left| \frac{\Delta V_{out}}{\Delta V_{CM}} \right| = \frac{\Delta R_D}{\frac{1}{g_m} + 2R_{SS}} \cdot \xrightarrow{R_{SS} >> 1/g_m} A_{CM-DM} \approx \frac{\Delta R_D}{2R_{SS}}.$$

Common mode (CM) to differential mode (DM) conversion

Common-Mode Rejection Ratio: CMRR

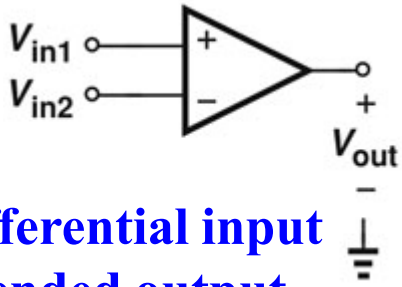


$$CMRR = \frac{A_{DM}}{A_{CM-DM}}$$

- **CMRR defines the ratio of wanted amplified differential input signal to unwanted converted input common-mode noise that appears at the output.**

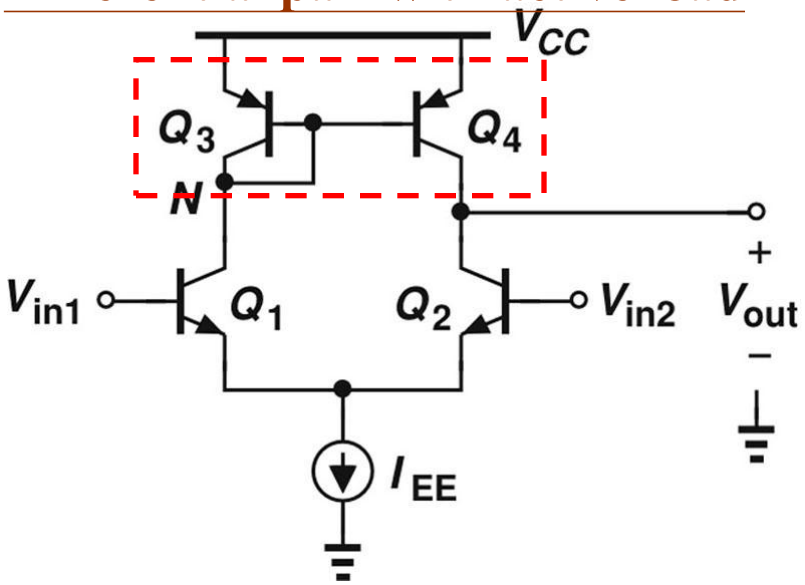
Differential to Single-ended Conversion

Op amp (Ch8)

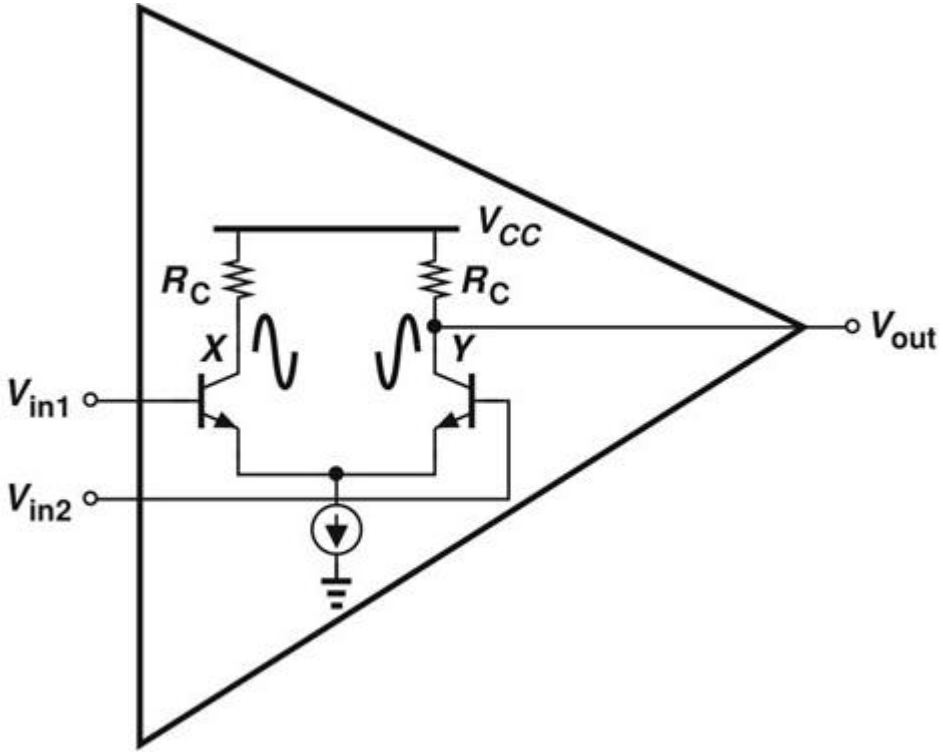


Convert differential input into single-ended output

Differential pair with active load



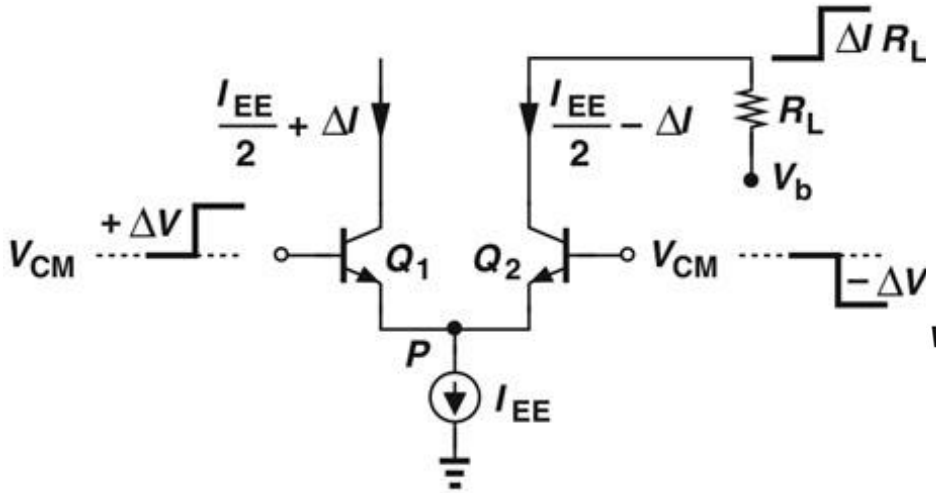
Possible implementation



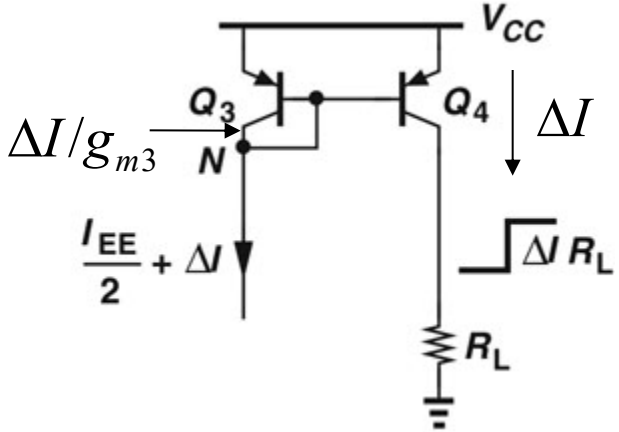
Voltage gain is halved!!

Qualitative Analysis

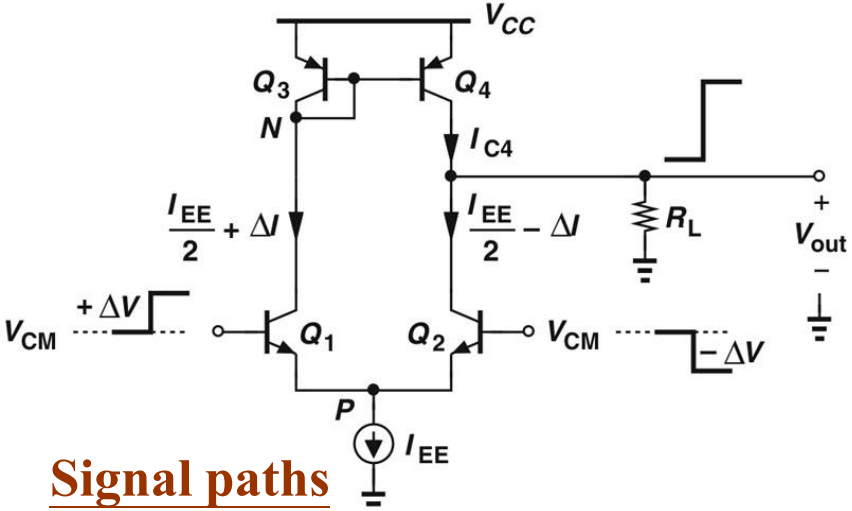
Response of input pair to input change



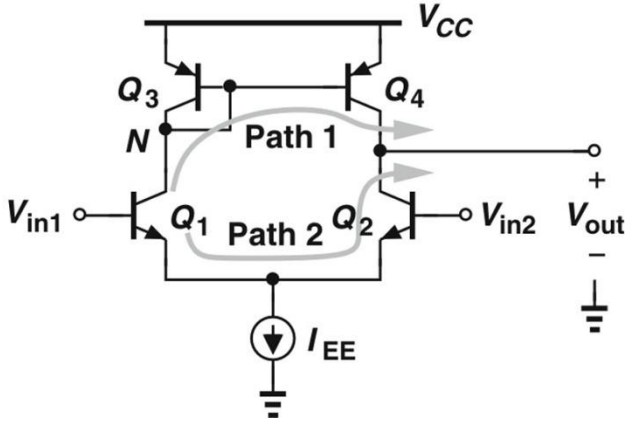
Response of active load to current change



Detailed operation



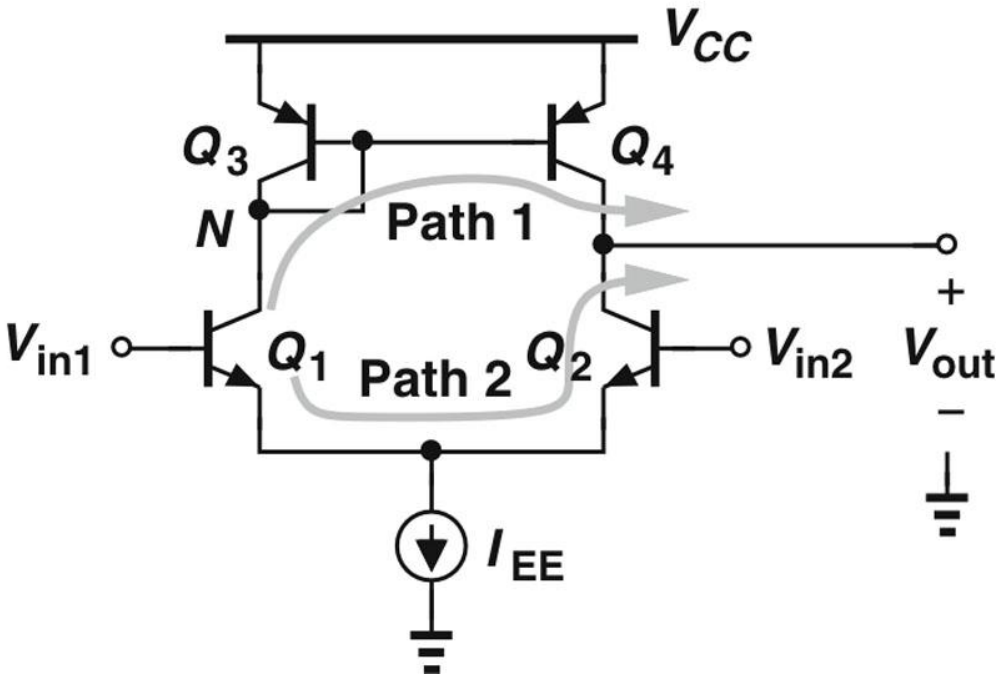
Signal paths



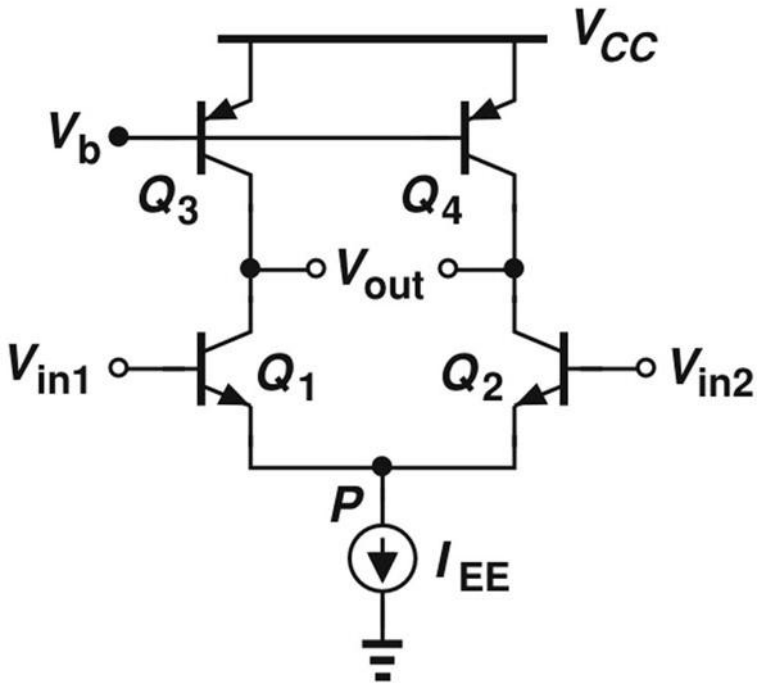
Current mirror carries signal!!

Active Load vs. Static Load

Active Load

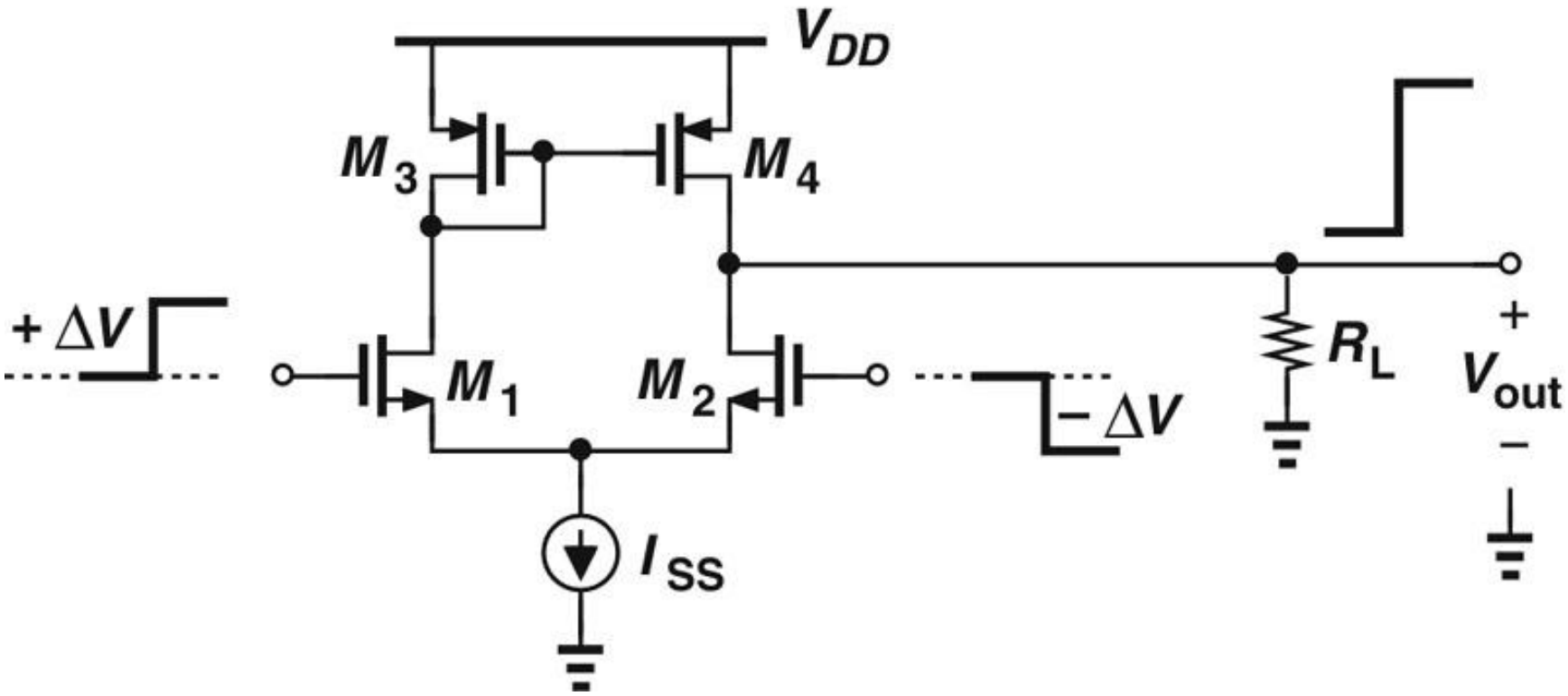


Static Load



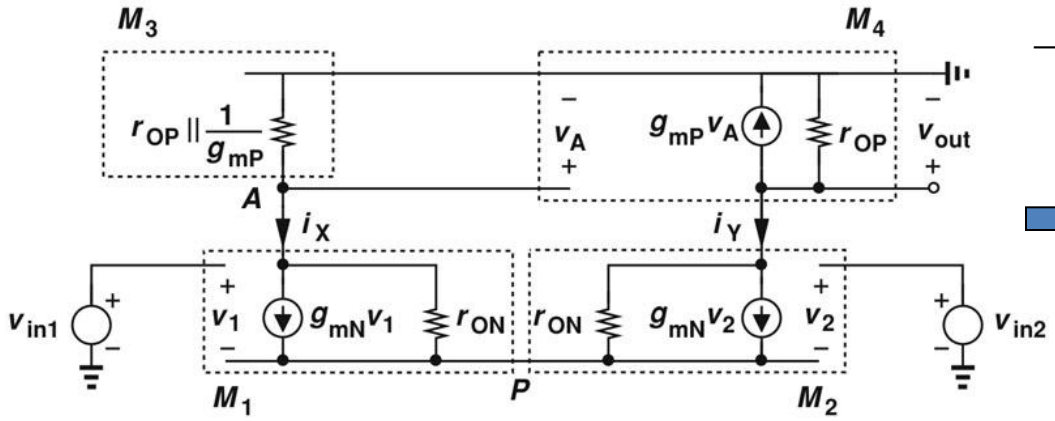
- **The load on the left responds to the input signal and enhances the single-ended output, whereas the load on the right does not.**

MOS Diff Pair with Active Load



- **Similar to its bipolar counterpart, MOS differential pair can also use active load to enhance its single-ended output.**

Small Signal Analysis



$$-v_A + (i_X - g_{mN}v_1)r_{ON} - (i_Y - g_{mN}v_2)r_{ON} + v_{out} = 0.$$

$$v_1 - v_2 = v_{in1} - v_{in2} \qquad i_X = -i_Y$$

$$\Rightarrow \quad -v_A + 2i_X r_{ON} - g_{mN}r_{ON}(v_{in1} - v_{in2}) + v_{out} = 0.$$

The circuit is asymmetric!!

***P* is not virtual ground!!**

$$\Rightarrow \quad \frac{v_{out}}{r_{OP}[1+g_{mP}(\frac{1}{g_{mP}} \| r_{OP})]}(\frac{1}{g_{mP}} \| r_{OP}) + 2r_{ON}\frac{v_{out}}{r_{OP}[1+g_{mP}(\frac{1}{g_{mP}} \| r_{OP})]}$$

$$+v_{out} = g_{mN}r_{ON}(v_{in1} - v_{in2}).$$

$$i_X = -i_Y \qquad v_A = -i_X(g_{mP}^{-1} \| r_{OP})$$

$$-i_Y = \frac{v_{out}}{r_{OP}} + g_{mP}v_A = \frac{v_{out}}{r_{OP}} - g_{mP}i_X(\frac{1}{g_{mP}} \| r_{OP}) = i_X.$$

$$\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN}r_{ON}\frac{r_{OP}[1+g_{mP}(\frac{1}{g_{mP}} \| r_{OP})]}{2r_{ON} + 2r_{OP}}.$$

$$\Rightarrow \quad i_X = \frac{v_{out}}{r_{OP}[1+g_{mP}(\frac{1}{g_{mP}} \| r_{OP})]}.$$

$$g_{mP}r_{oP} >> 1 \quad \Rightarrow \quad \boxed{\frac{v_{out}}{v_{in1} - v_{in2}} = g_{mN}(r_{ON} \| r_{OP}).}$$

Designer's Intuition

- Simulation is essential because the behavior of short-channel MOSFET can't be predicted accurately by hand calculations.
- Don't avoid a simple and intuitive analysis of the circuit and skip the task of gaining inside, you can't interpret the simulate results intelligently.
- Don't let the computer think for you!